

Welcome To

ISSCC 2014
Session 24
Integrated Biomedical Systems



A Miniaturized 64-channel, 225μW Wireless Electrocorticographic Neural Sensor

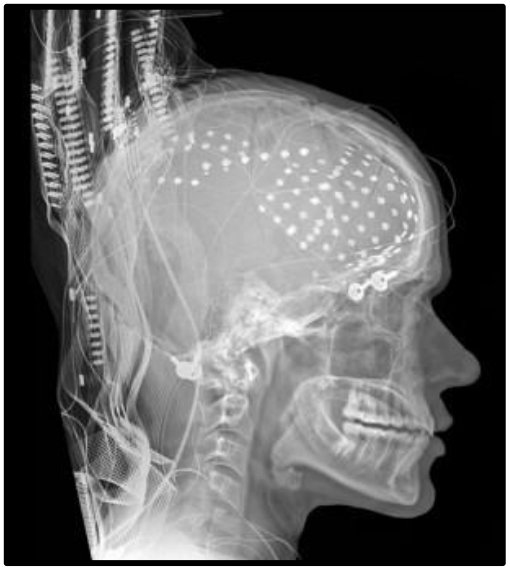
Rikky Muller[1,2], Hanh-Phuc Le[1], Wen Li[1], Peter Ledochowitsch[1], Simone Gambini[2], Toni Bjorninen[3], Aaron Koralek[1], Jose M. Carmena[1], Michel M. Maharbiz[1], Elad Alon[1], Jan M. Rabaey[1]

[1]University of California, Berkeley, Berkeley, CA
[2]University of Melbourne, Melbourne, Australia
[3]Tampere University of Technology, Tampere, Finland

International Solid-State Circuits Conference
San Francisco, CA
February 9, 2014

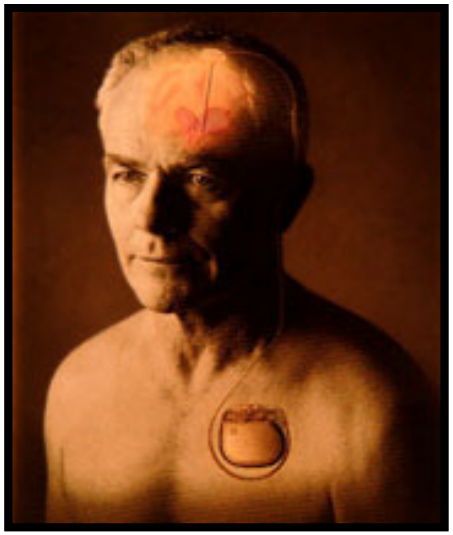
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Neural Interfaces



PRE-SURGICAL MAPPING

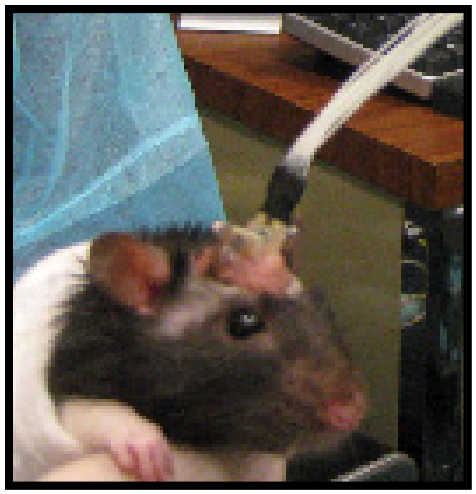




DISEASE THERAPIES



MOTOR PROSTHETICS



BEHAVIORAL NEUROSCIENCE



SPEECH PROSTHETICS

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Past and Future Interfaces



Hochberg, *Nature* ‘12

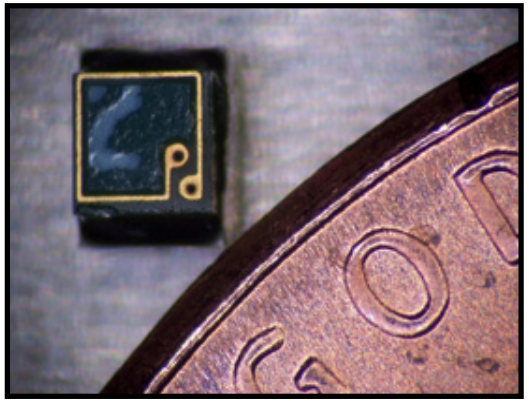
TODAY’S DEVICES



Past and Future Interfaces



Hochberg, *Nature* '12

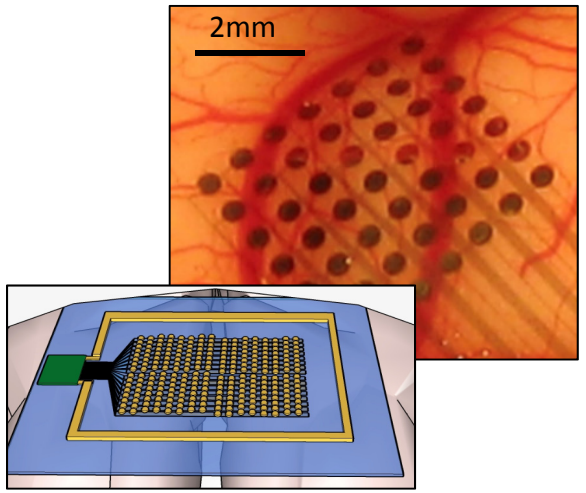


Mark, *VLSI* '11

TODAY'S DEVICES



TOMORROW'S DEVICES

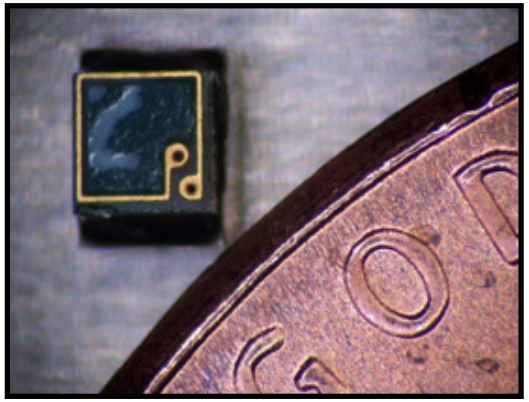


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Past and Future Interfaces

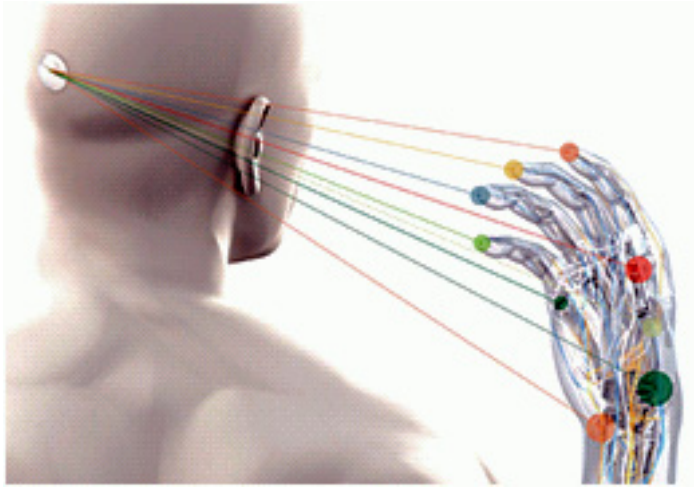


Hochberg, *Nature* '12



Mark, *VLSI* '11

THE VISION

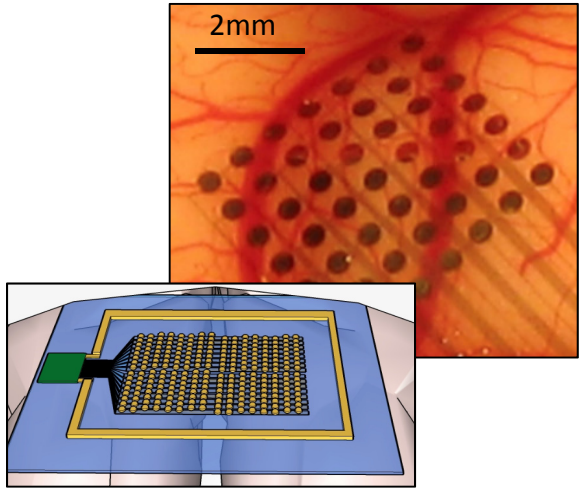


Carmena, *IEEE Spectrum* '12

TODAY'S DEVICES

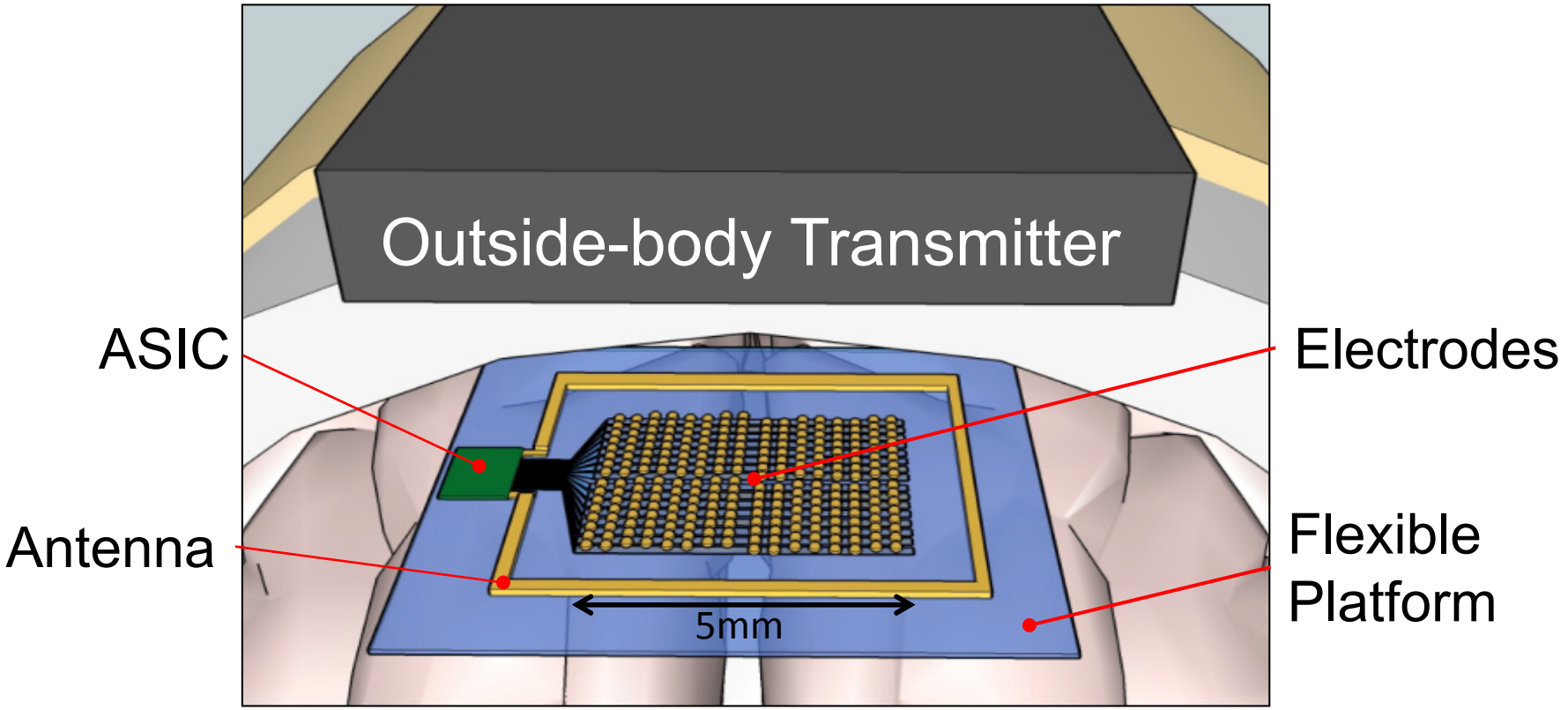


TOMORROW'S DEVICES



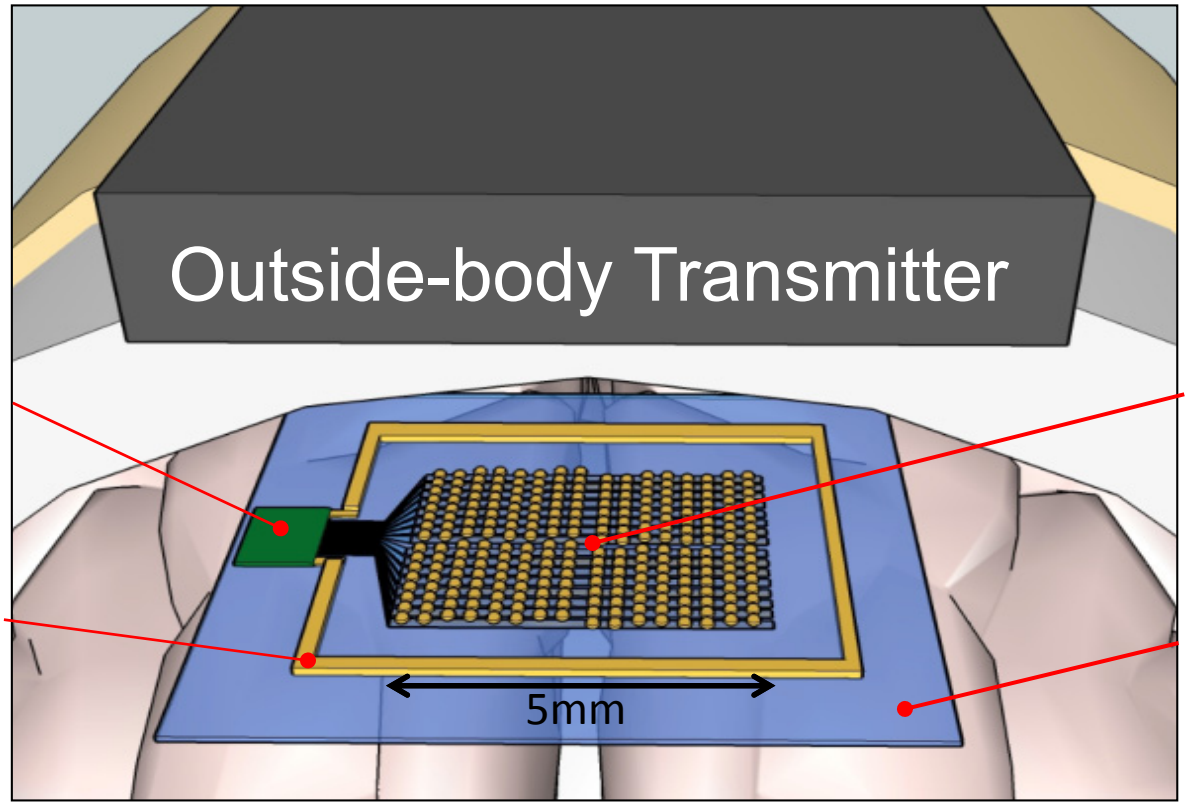
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Implantable μECoG



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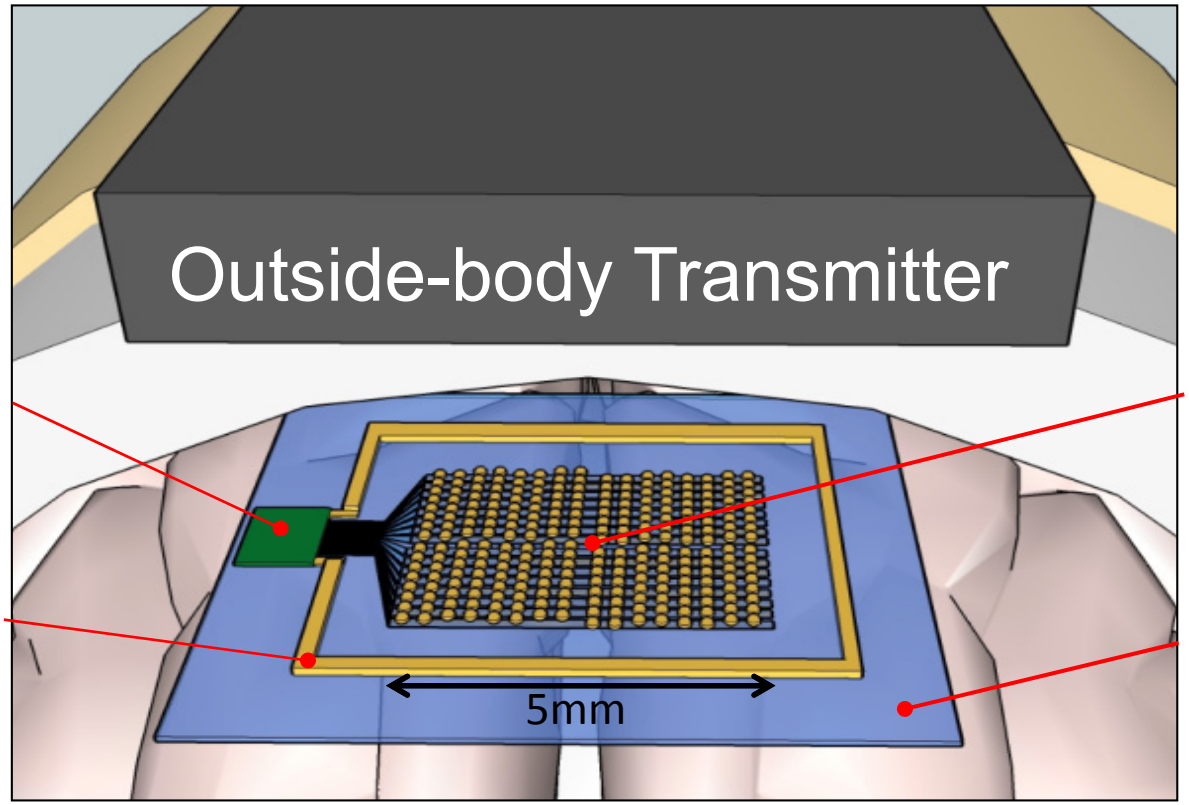
Implantable μECoG



✓ Non-penetrating flexible array → *no cortical scarring*

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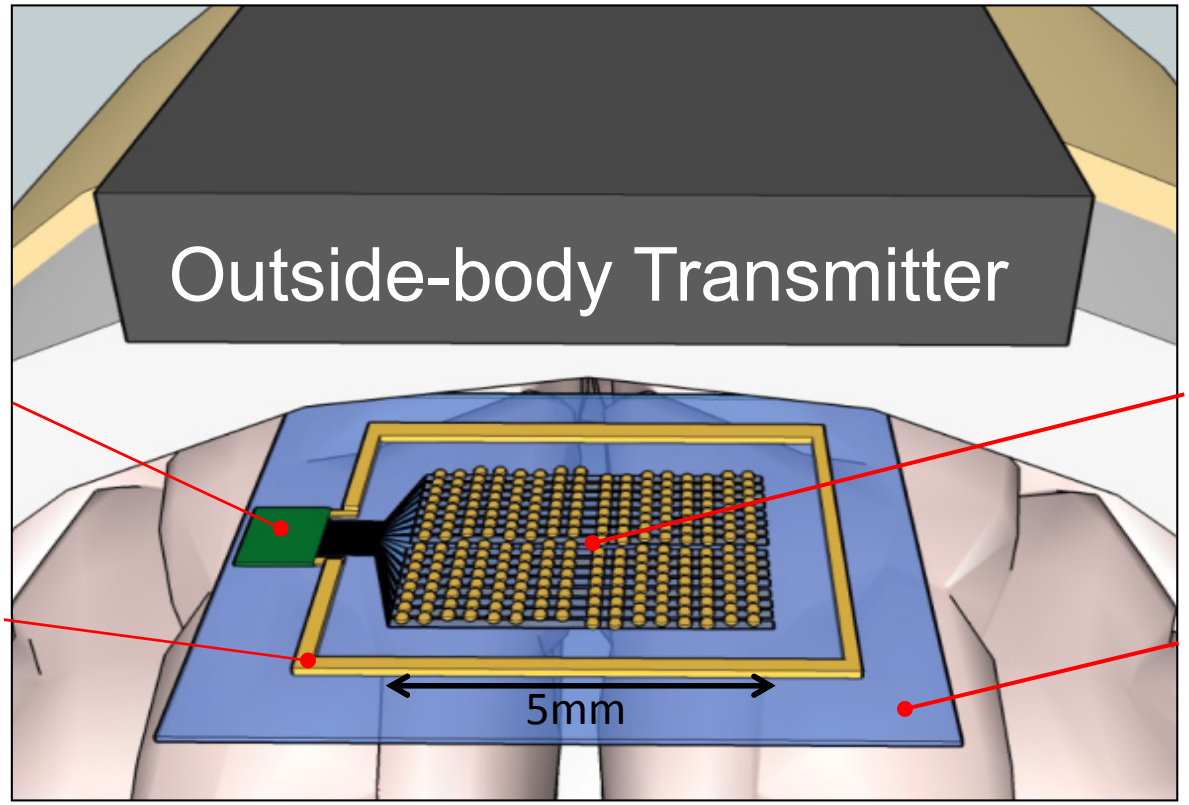
Implantable μECoG



- ✓ Non-penetrating flexible array → *no cortical scarring*
- ✓ Fully wireless and implantable → *minimal infection risk*

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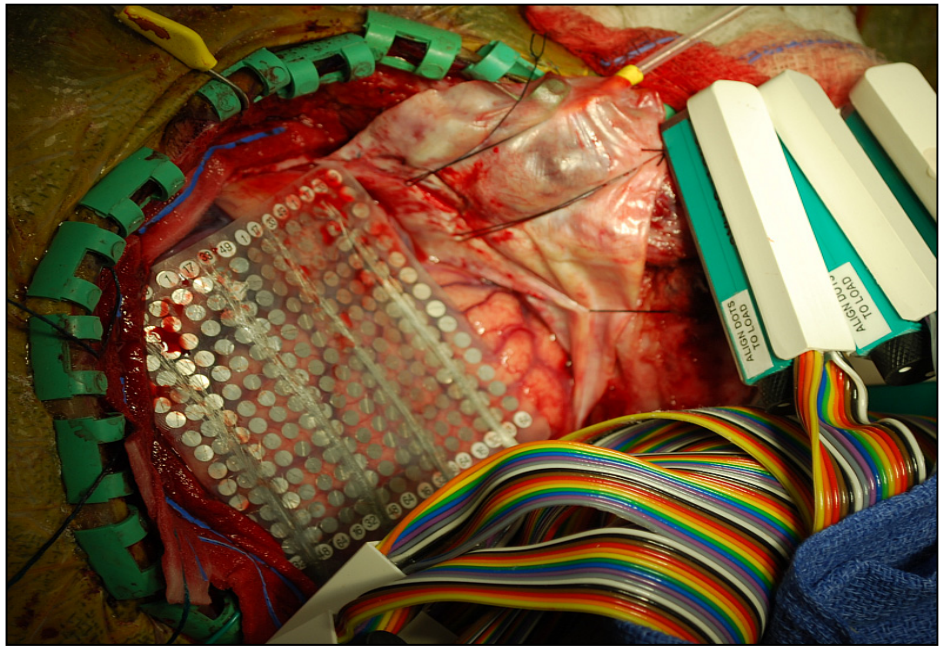
Implantable μECoG

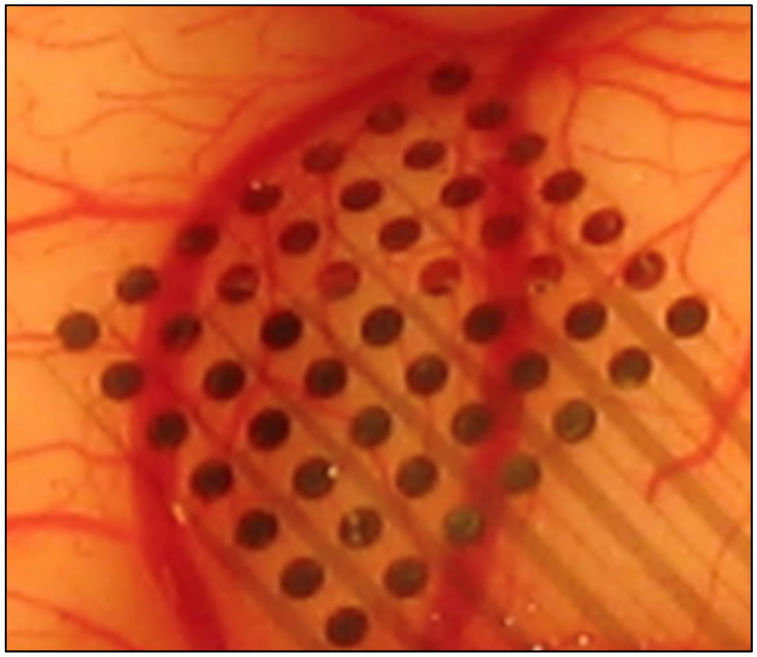


- ✓ Non-penetrating flexible array → *no cortical scarring*
- ✓ Fully wireless and implantable → *minimal infection risk*
- ✓ Fully integrated, low area IC → *reduced foreign body response*
- ✓ Low-power IC → *safe RF energy levels for chronic use*

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High-Density Electrodes

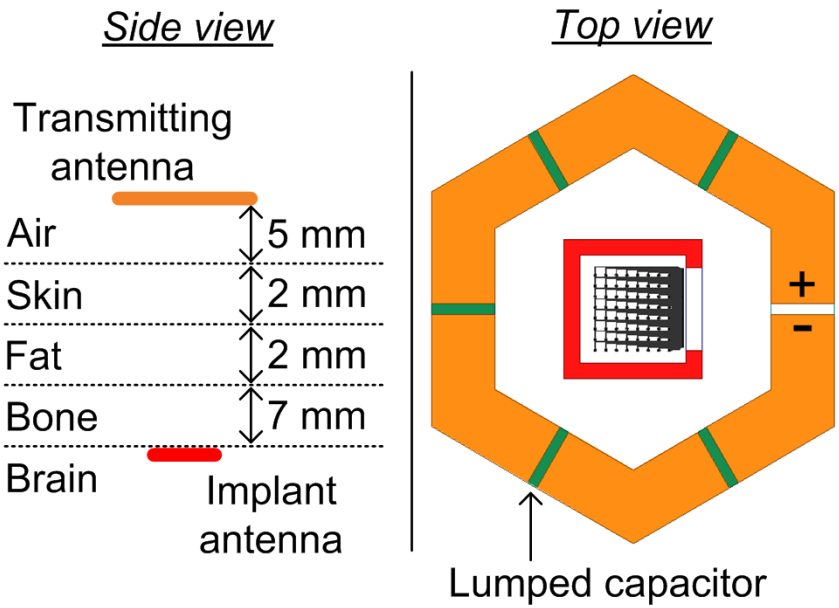


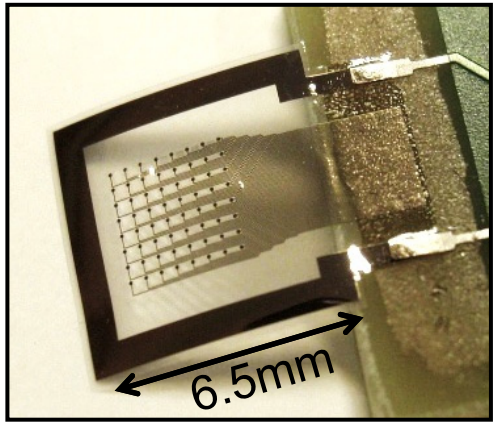


	AD-TECH MEDICAL	Ledochowitsch, *MEMS* '12
Material	Silicone, Platinum	Parylene C, Gold, Platinum
Assembly	Spot weld	Microfabrication
Pitch	4mm +	0.5mm
Connection	Cables	Direct bonding to Circuitry
Implantation	Craniotomy	Burr-hole

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Link Modeling and Safety

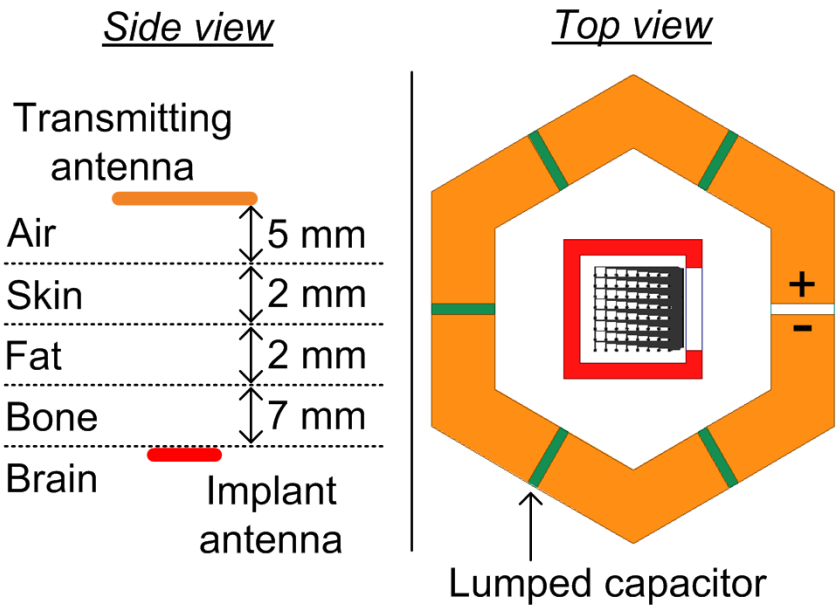


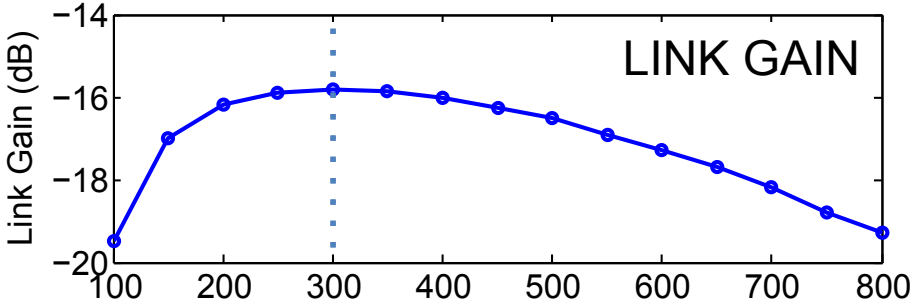


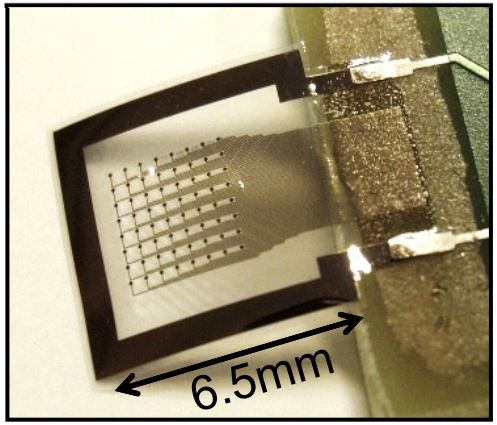
Bjorninen, *AWPL* '13

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Link Modeling and Safety



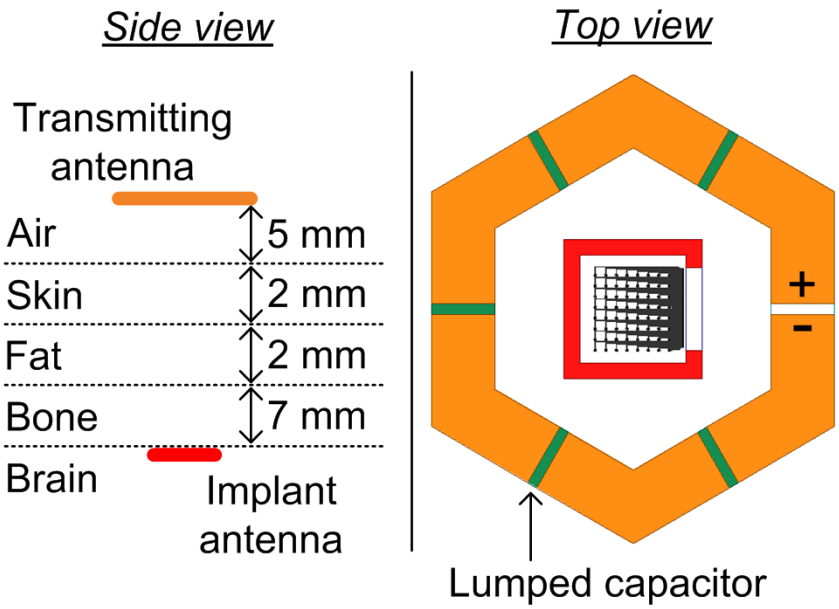


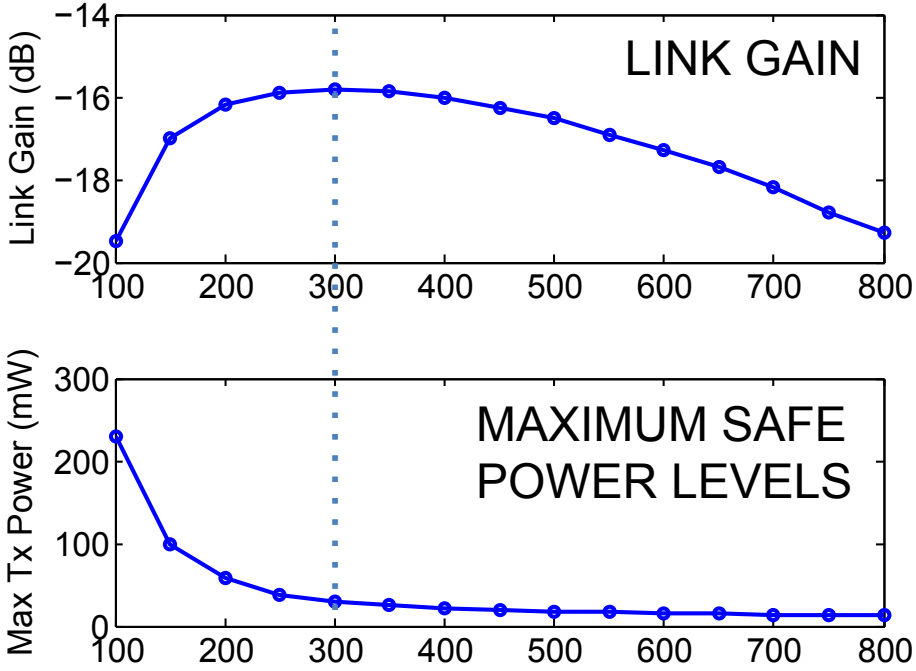


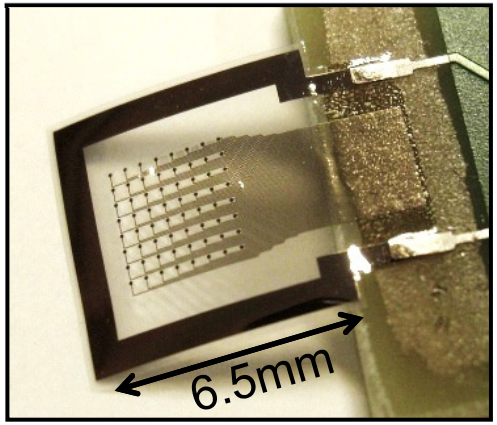
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Link Modeling and Safety



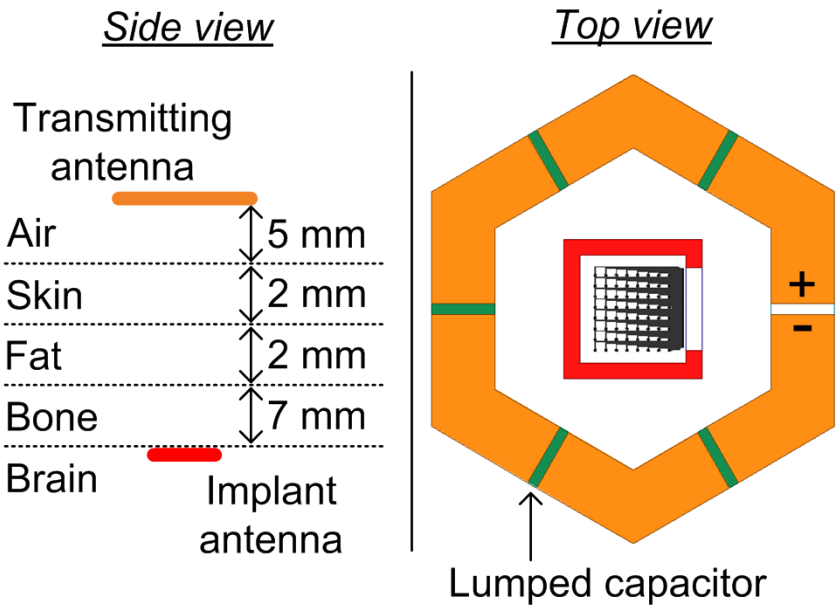


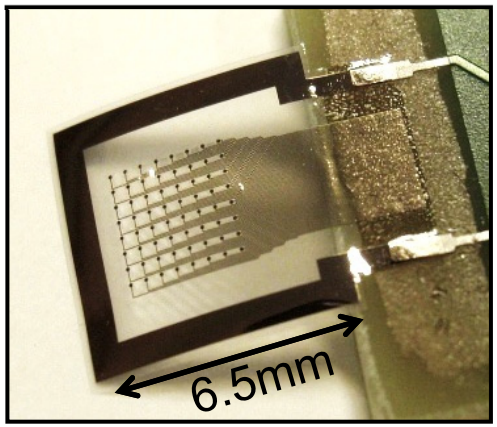


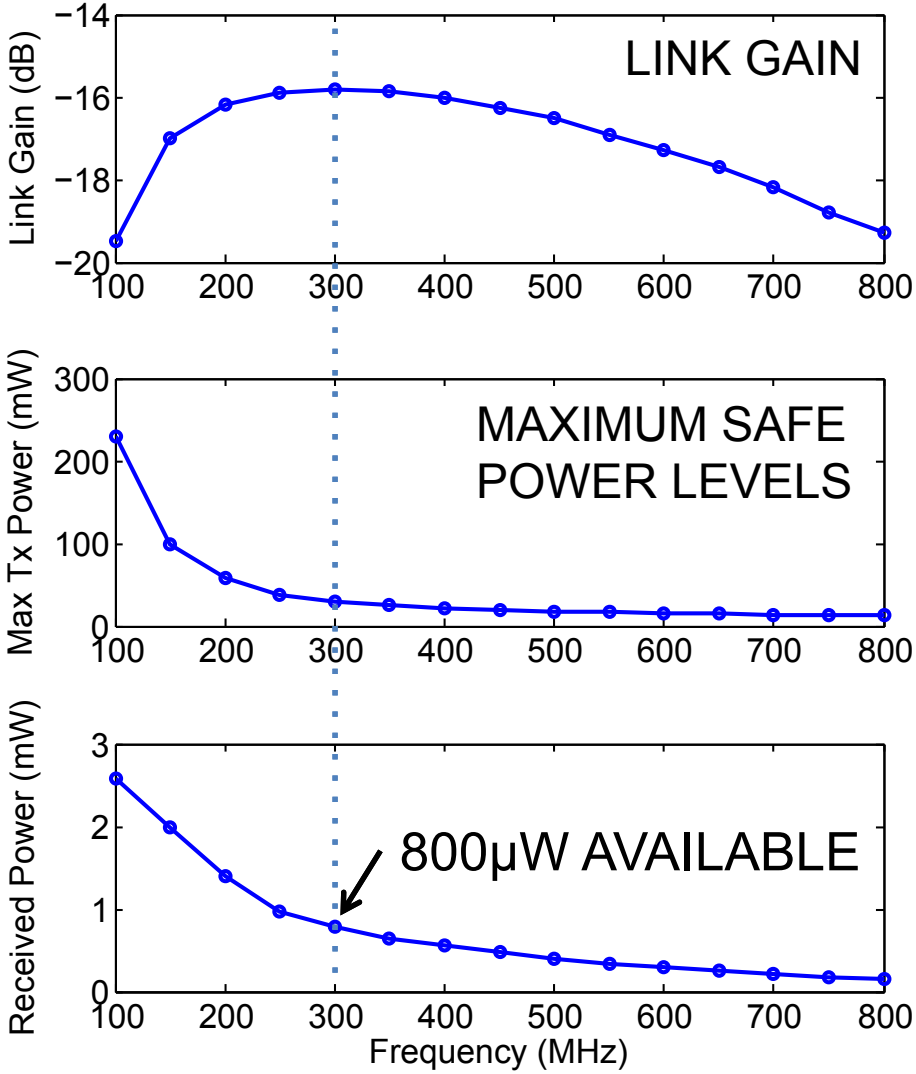
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Link Modeling and Safety



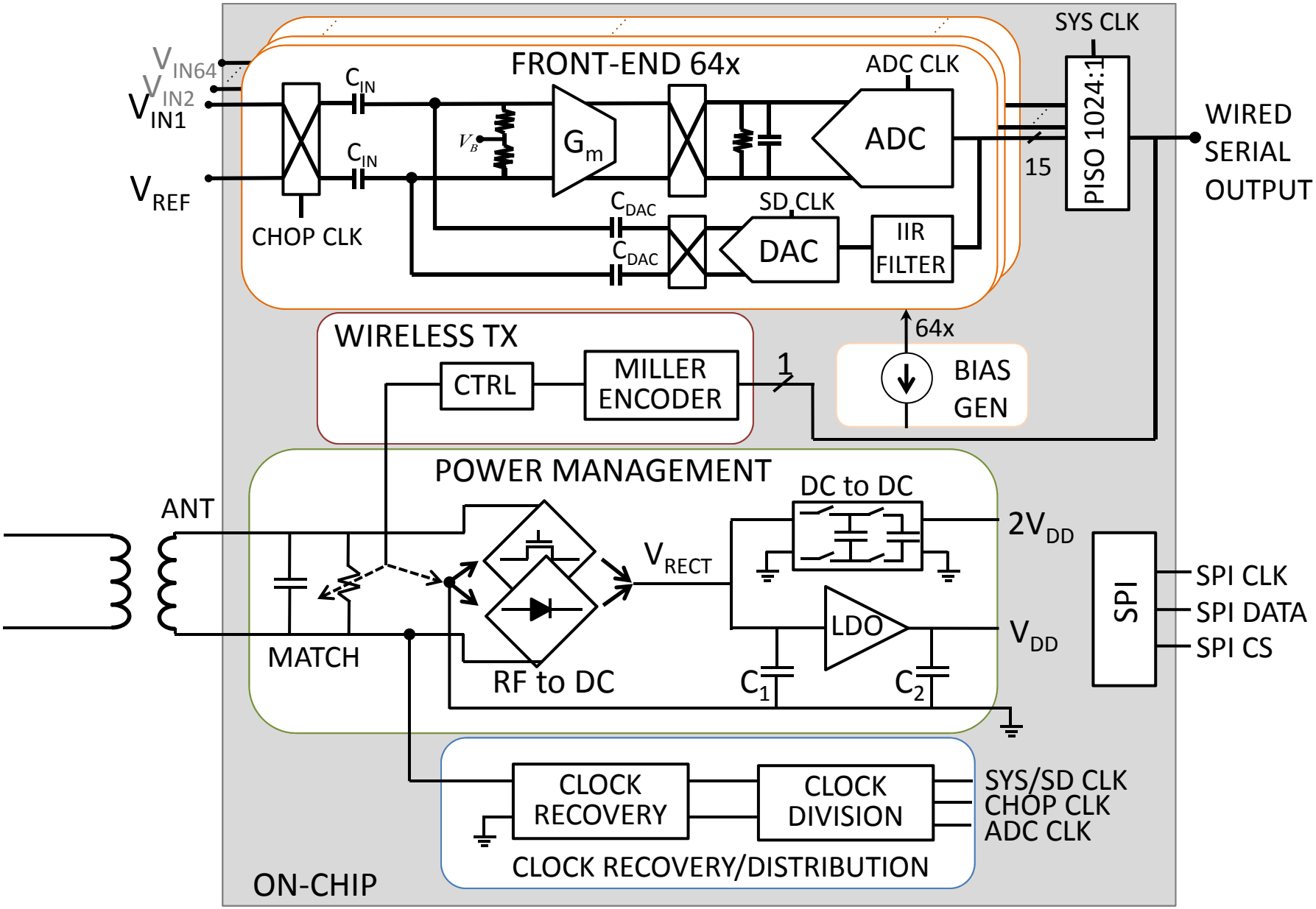




Bjorninen, *AWPL* '13

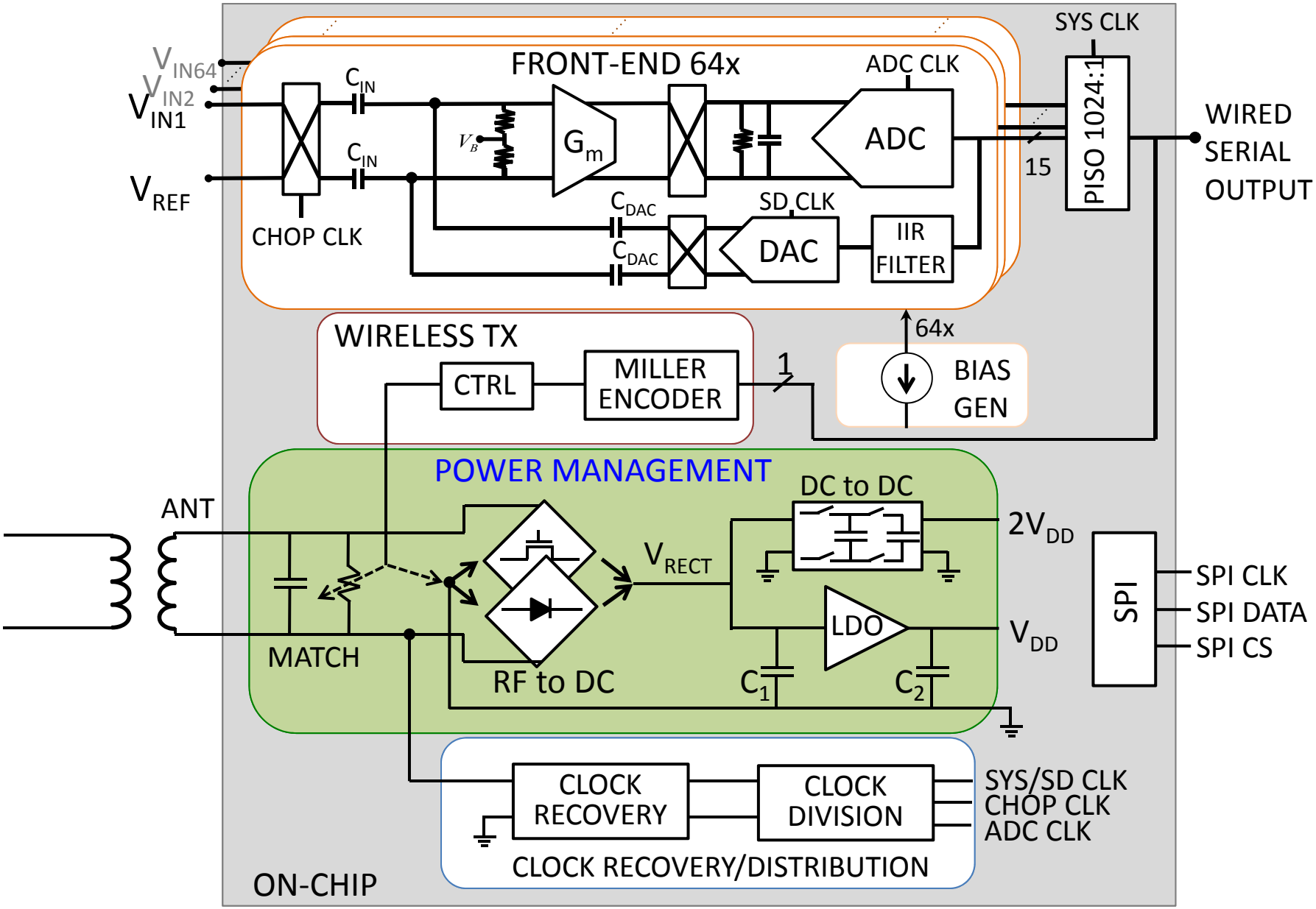
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IC Block Diagram



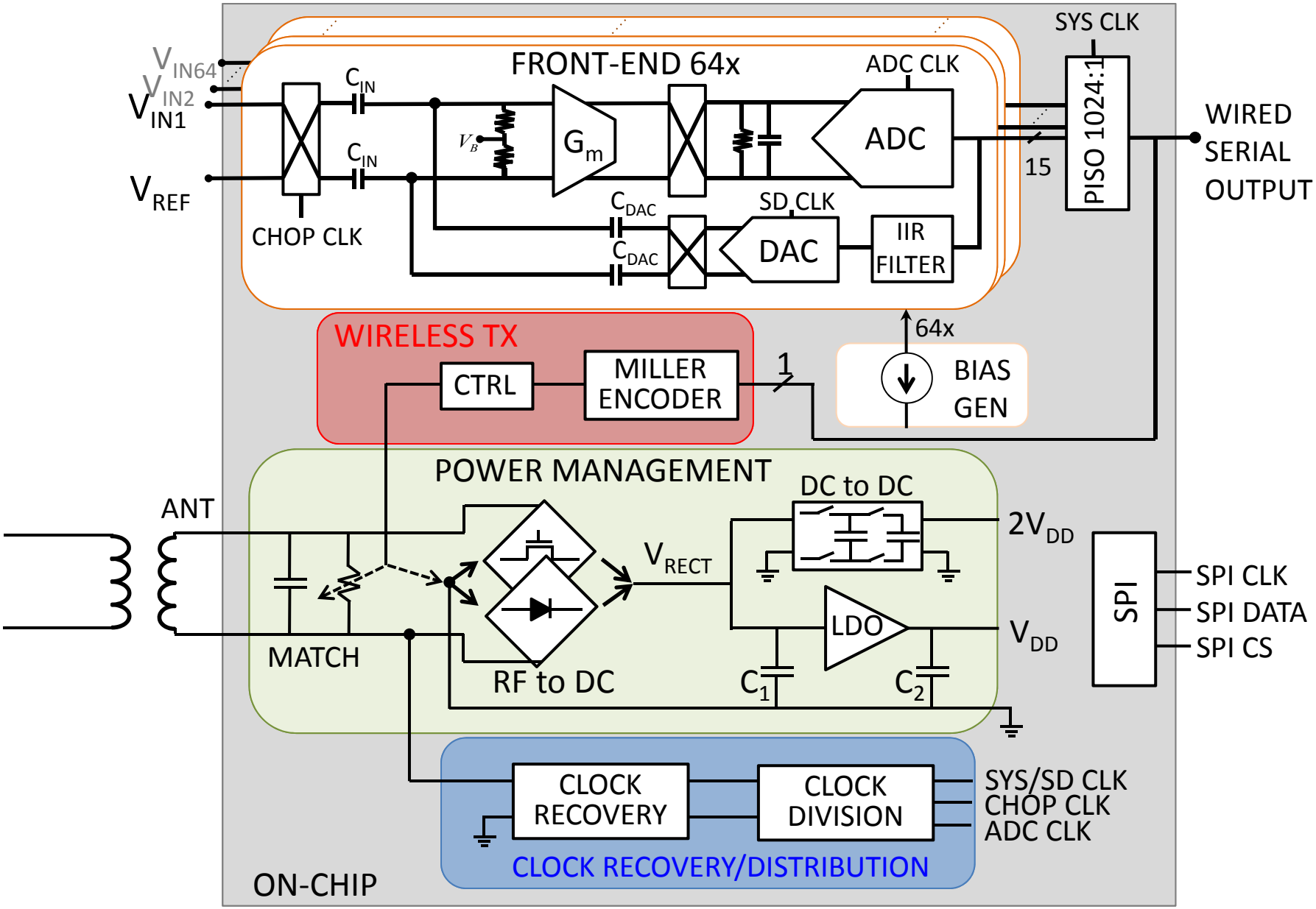
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IC Block Diagram



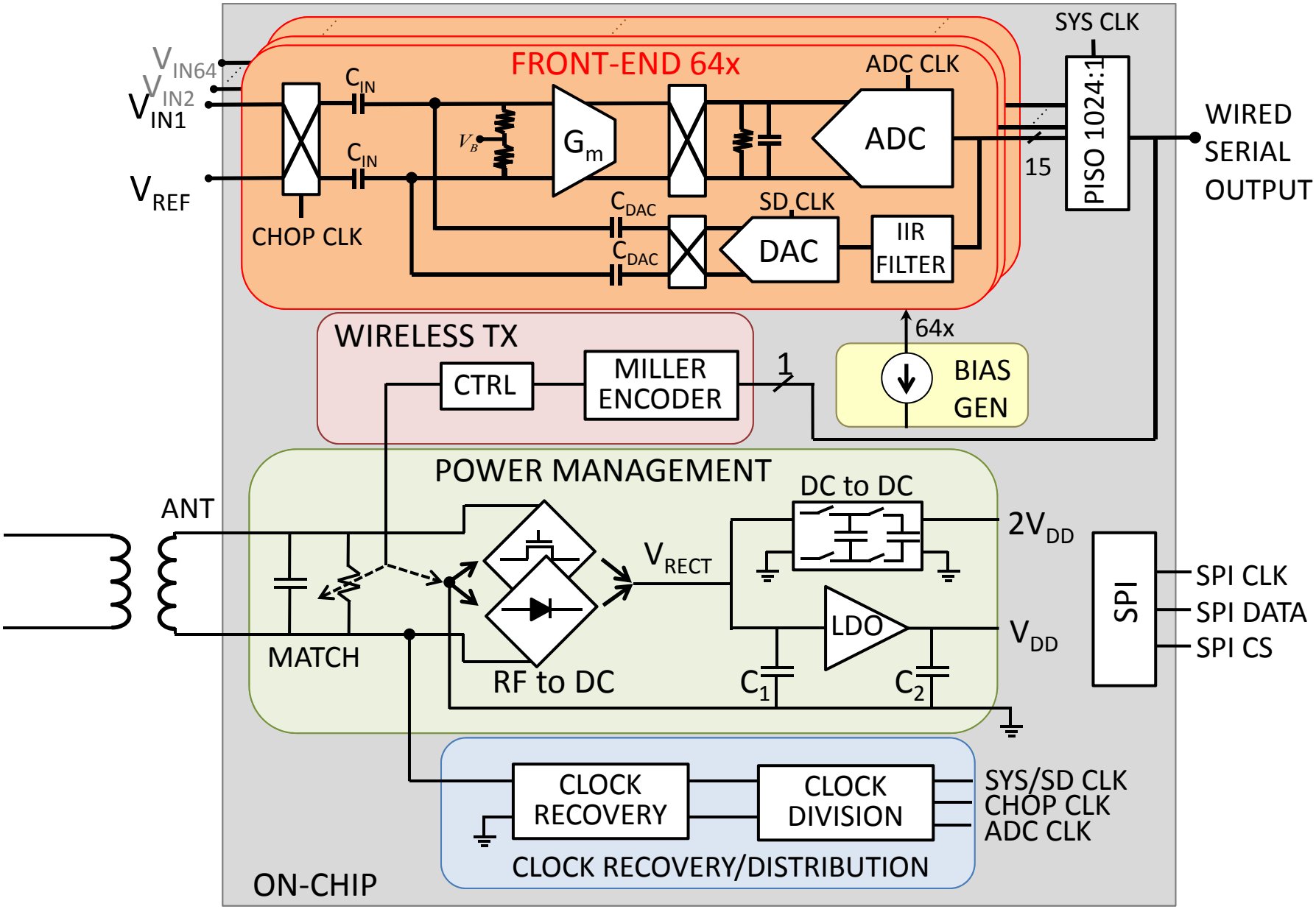
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IC Block Diagram



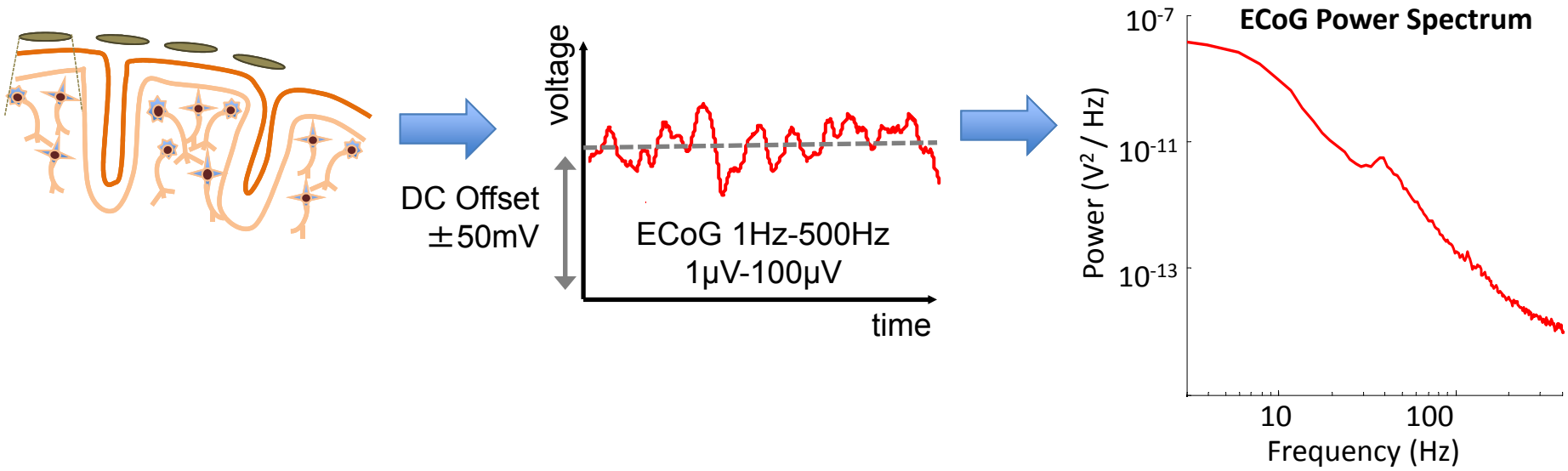
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IC Block Diagram



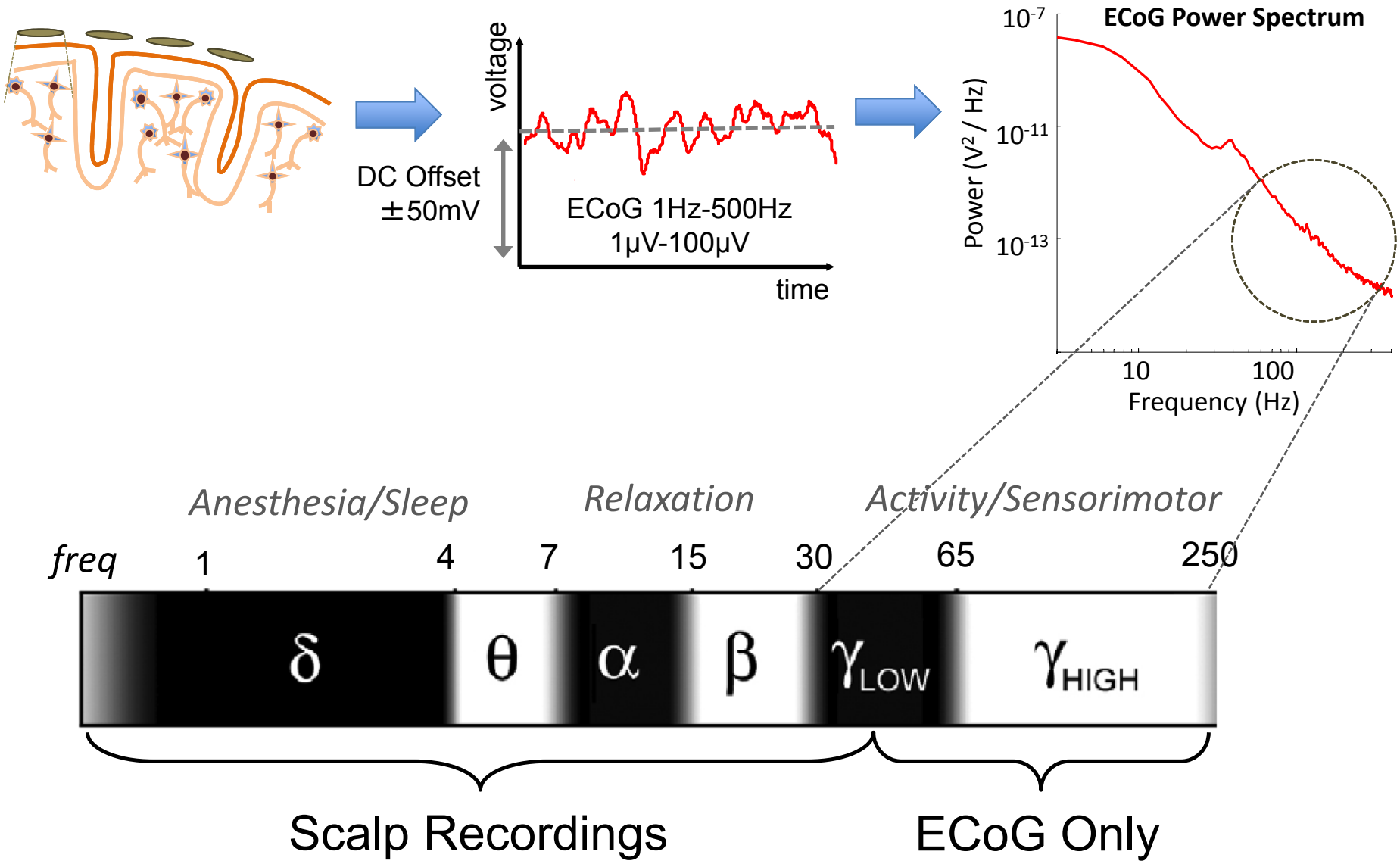
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Front-End Architecture



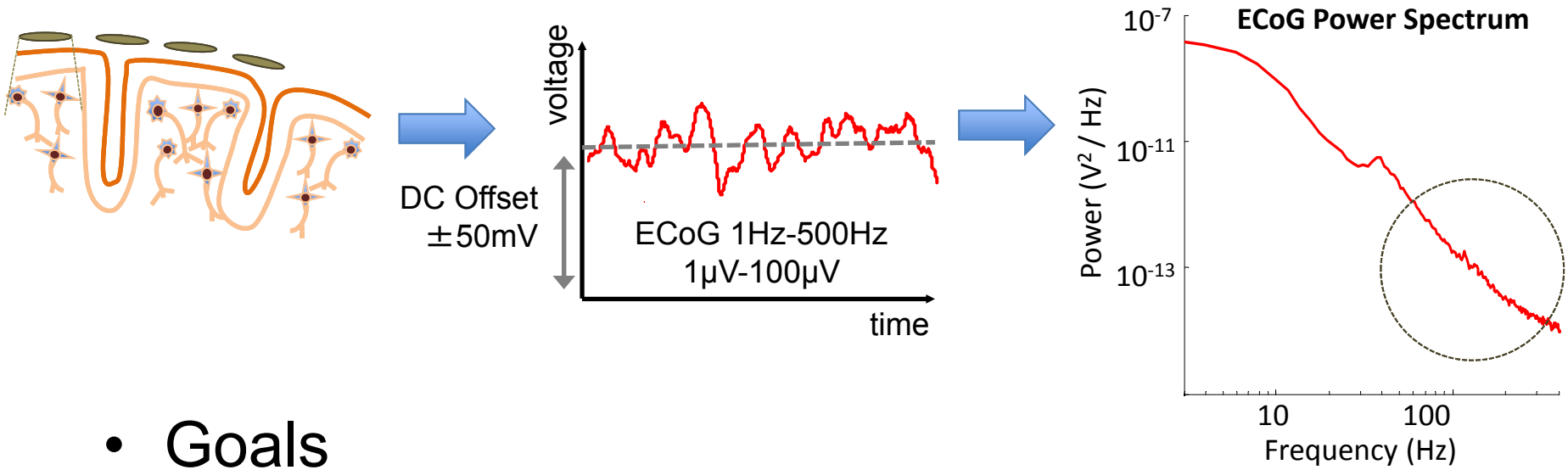
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Front-End Architecture



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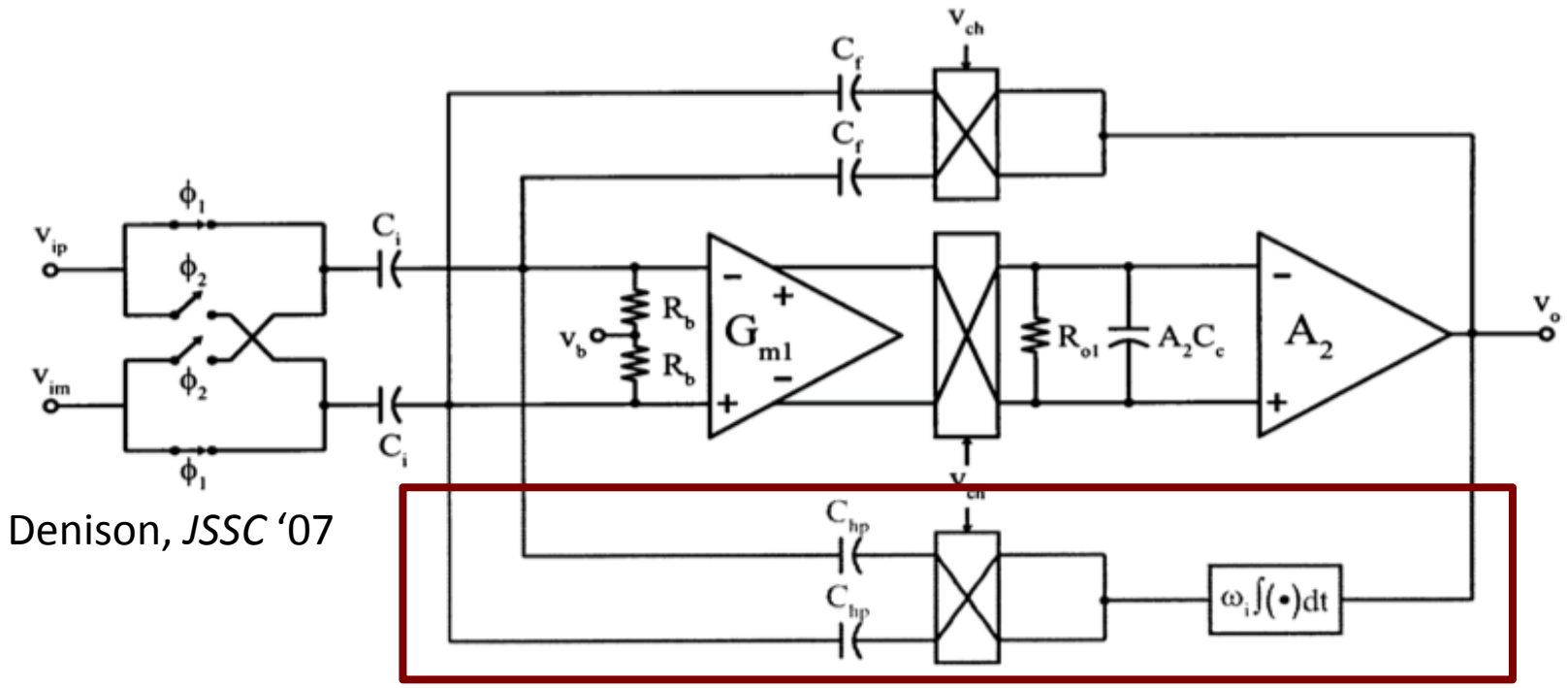
Front-End Architecture



- Goals
 - Eliminate DC Offset
 - Amplification and Analog to Digital Conversion
- Challenges
 - Low Frequency → 1/f Noise Reduction
 - Low SNR at input → Low Input-referred Noise
 - Low Power, Area

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State of the Art

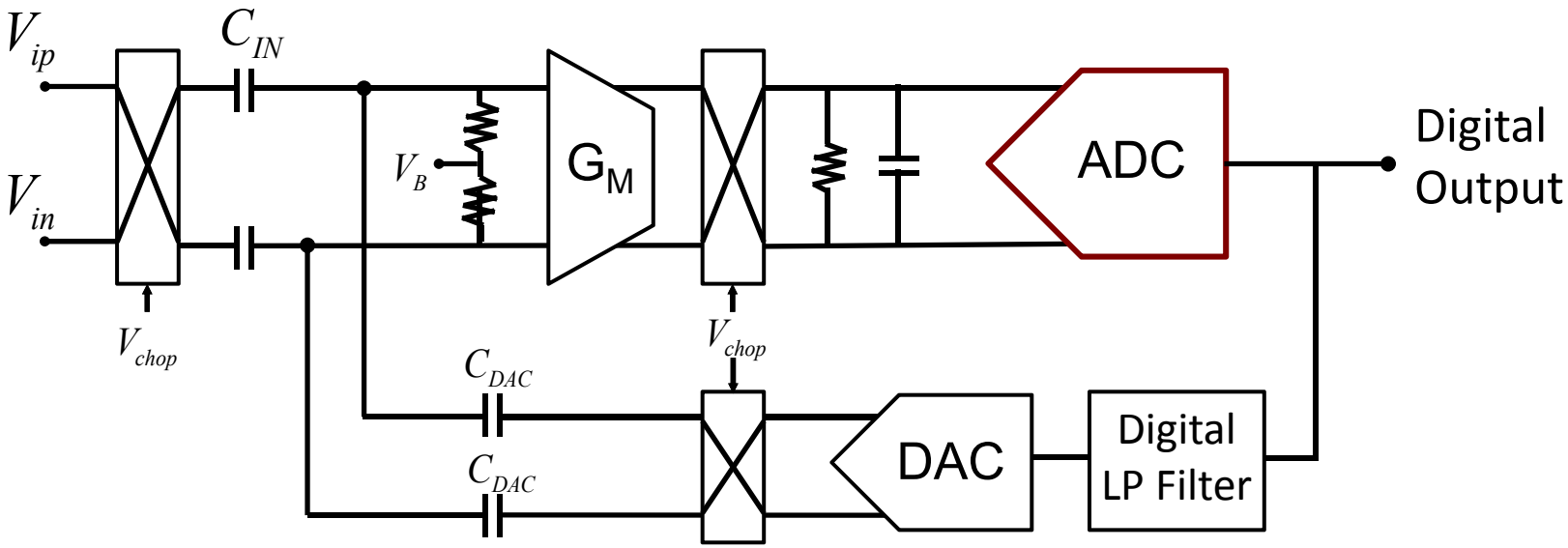


Denison, *JSSC* '07

- Chopper stabilized instrumentation amplifier
 - Upmodulates input & electrode offset
 - Cancelled through DC feedback loop
 - **Large (~nF) capacitors required for filtering**

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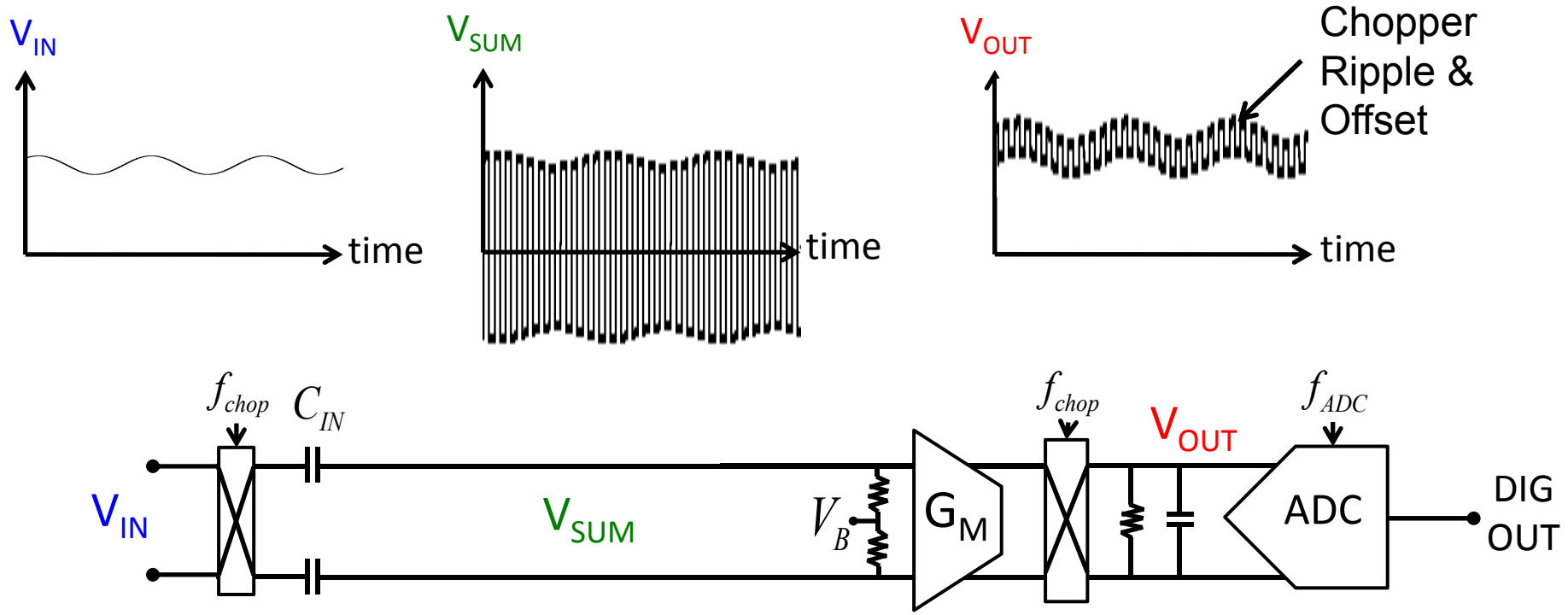
Front-End Architecture



- Move filter into the digital domain
 - Offset cancelled through **mixed-signal feedback loop**
 - **Small capacitors** required for signal combination

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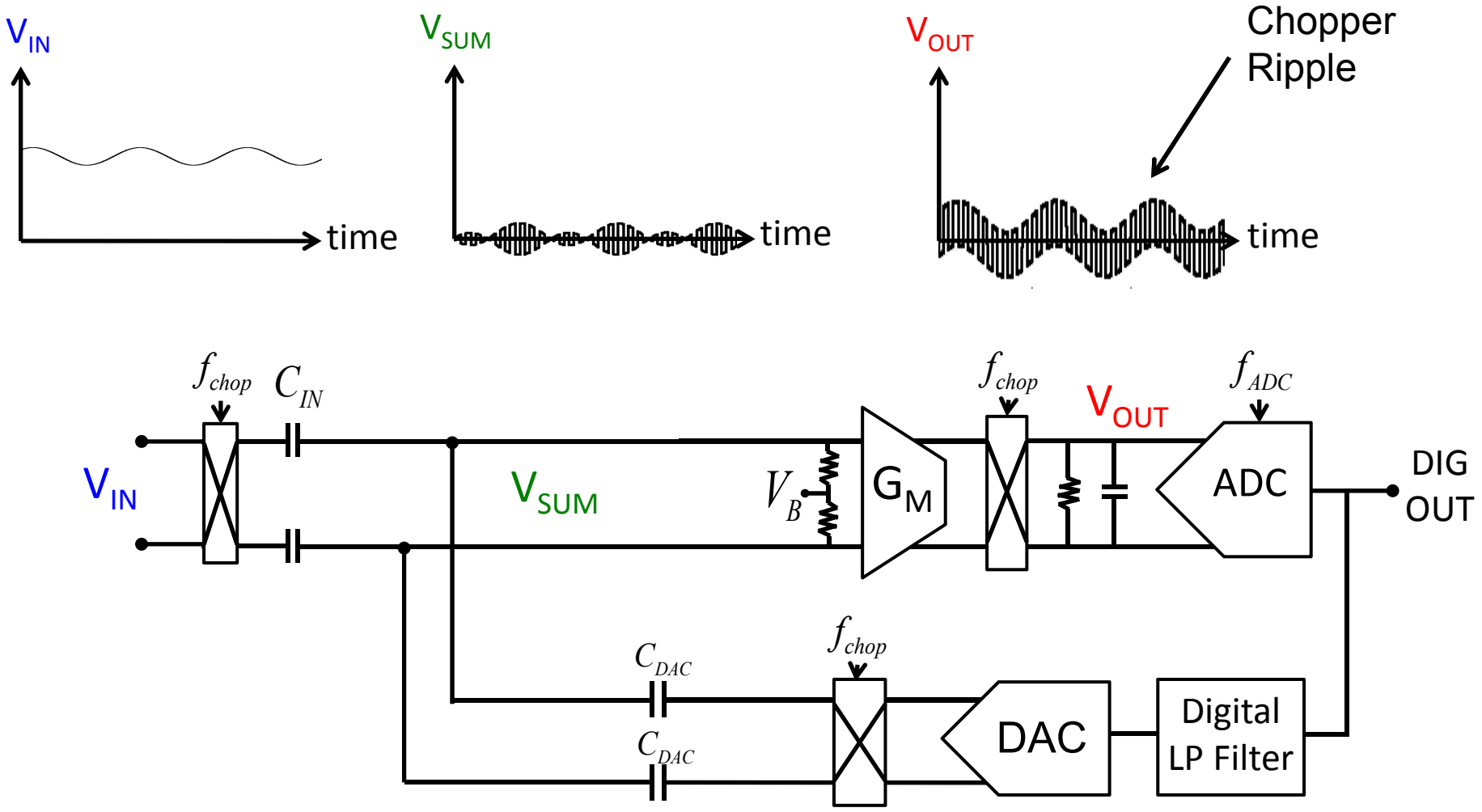
Front-End Operation



- Chopper stabilization upmodulates electrode offset
 - Offset still present at output → Saturate electronics

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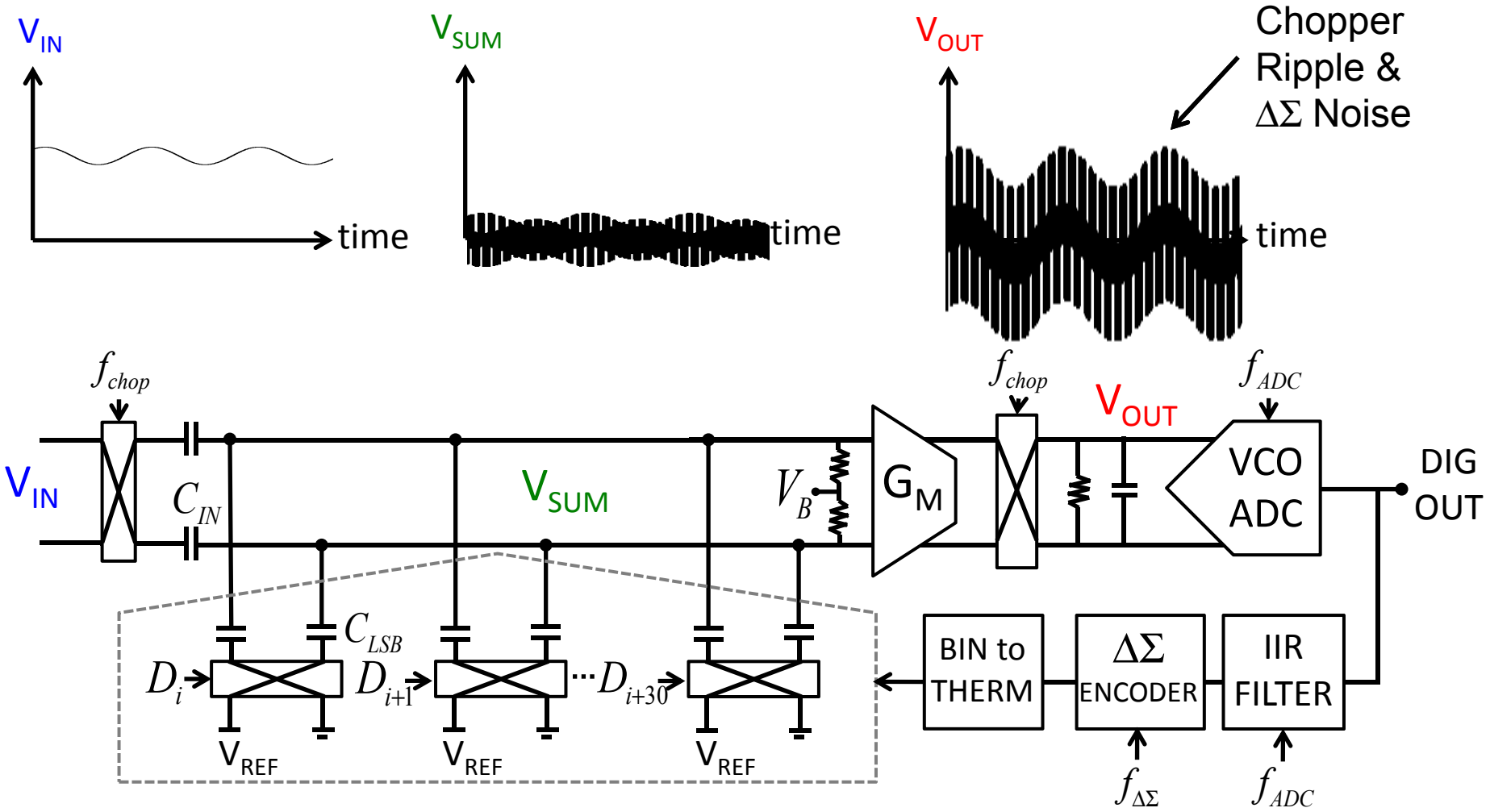
Front-End Operation



- DAC quantization noise < thermal noise
 - At least 16 bits required → Large DAC area

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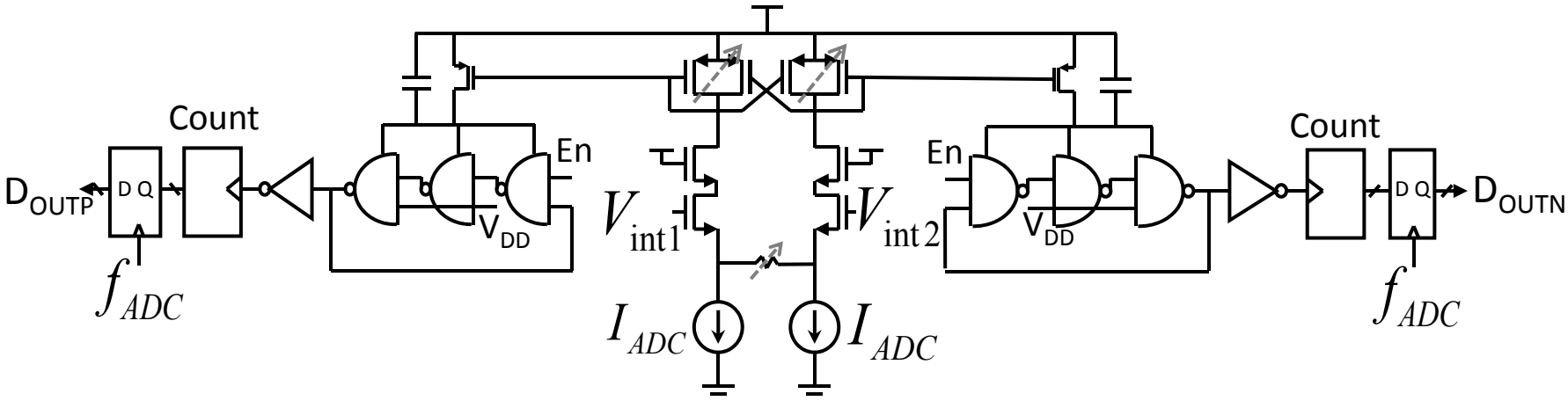
Front-End Operation

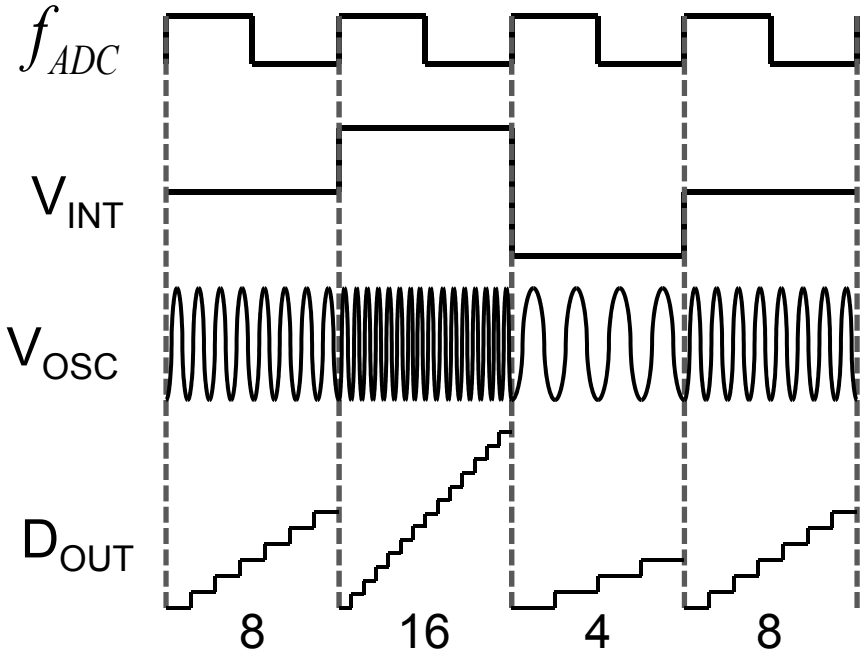


- Achieve high-resolution with ΔΣ DAC, 1000x OSR
 - 5 physical bits required to minimize V_{SUM} swing

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VCO-Based ADC



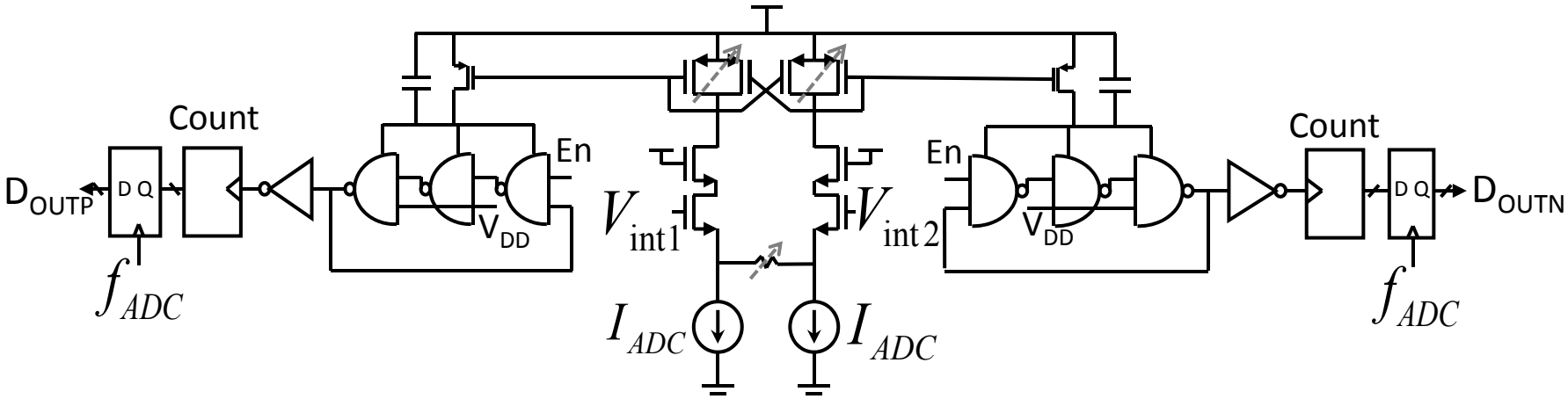


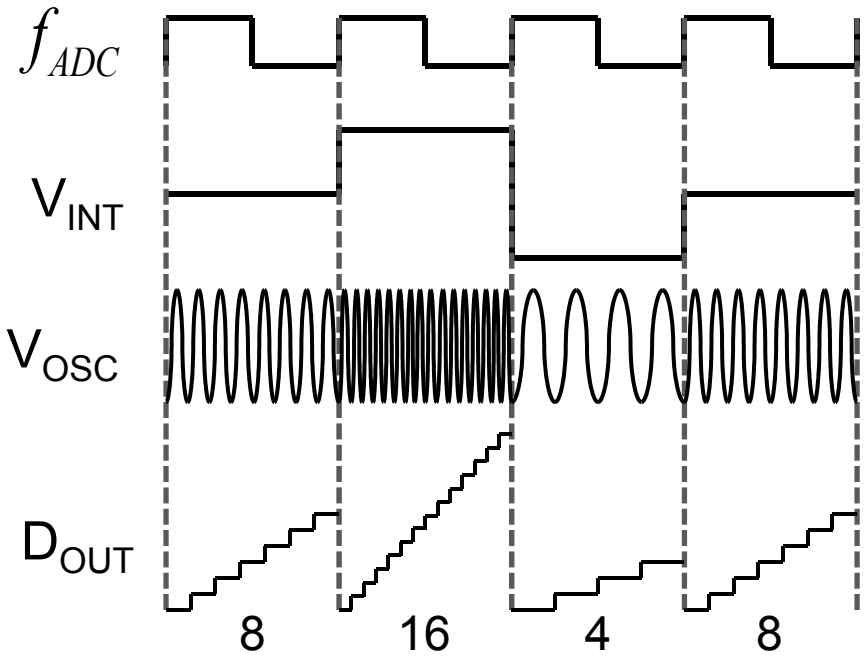
Muller, *ISSCC* '11

- 1kS/s, 15-bit ADC
- Low gain requirement
- Mostly digital
 - low energy/conv. step
- Suppresses chopper ripple & $\Delta\Sigma$ noise

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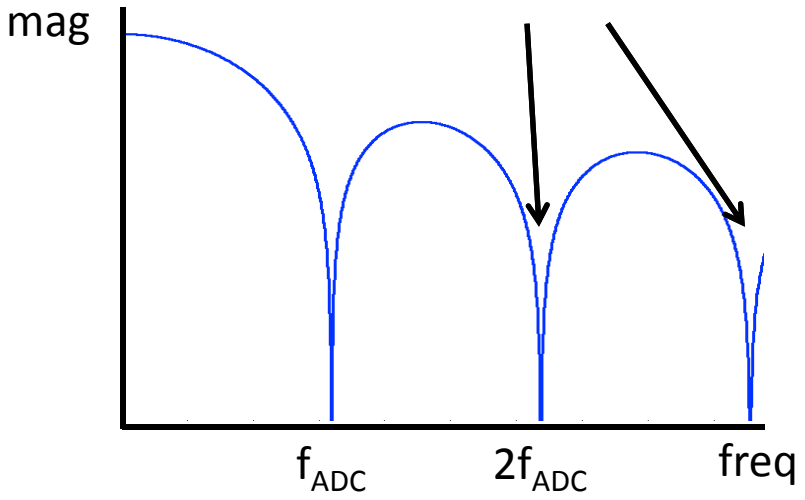
VCO-Based ADC





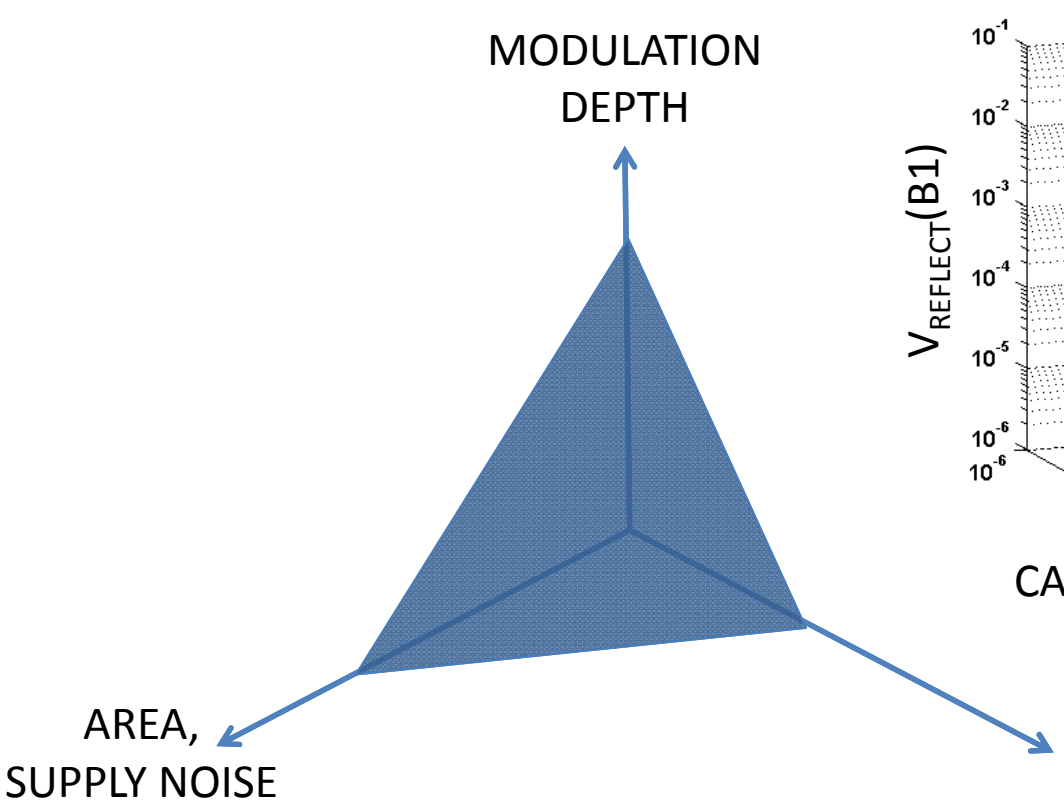
Muller, *ISSCC* '11

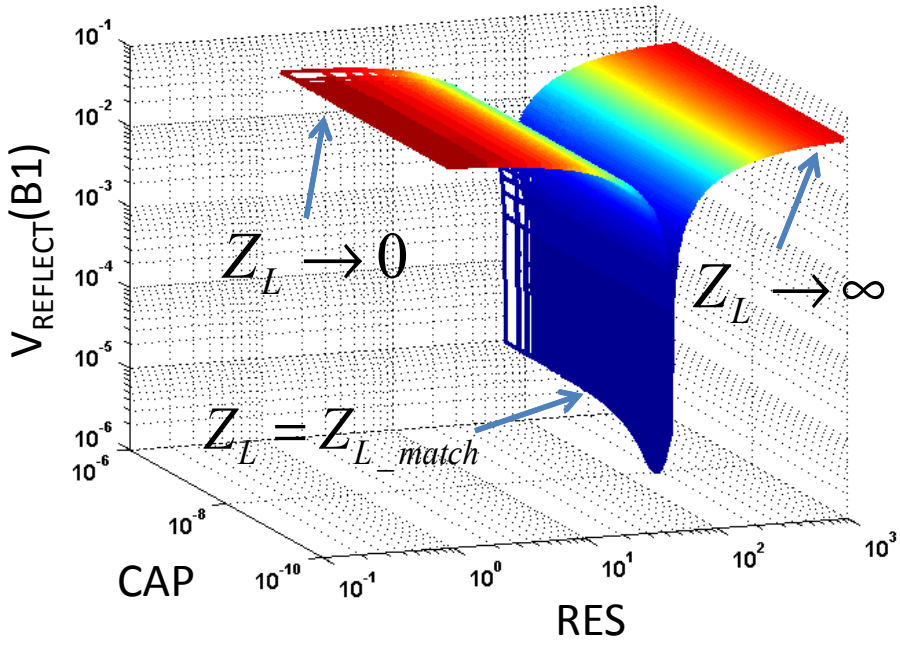
- Sinc transfer function
 - Design $f_{\Delta\Sigma}$ & f_{CHOP} at ADC harmonics



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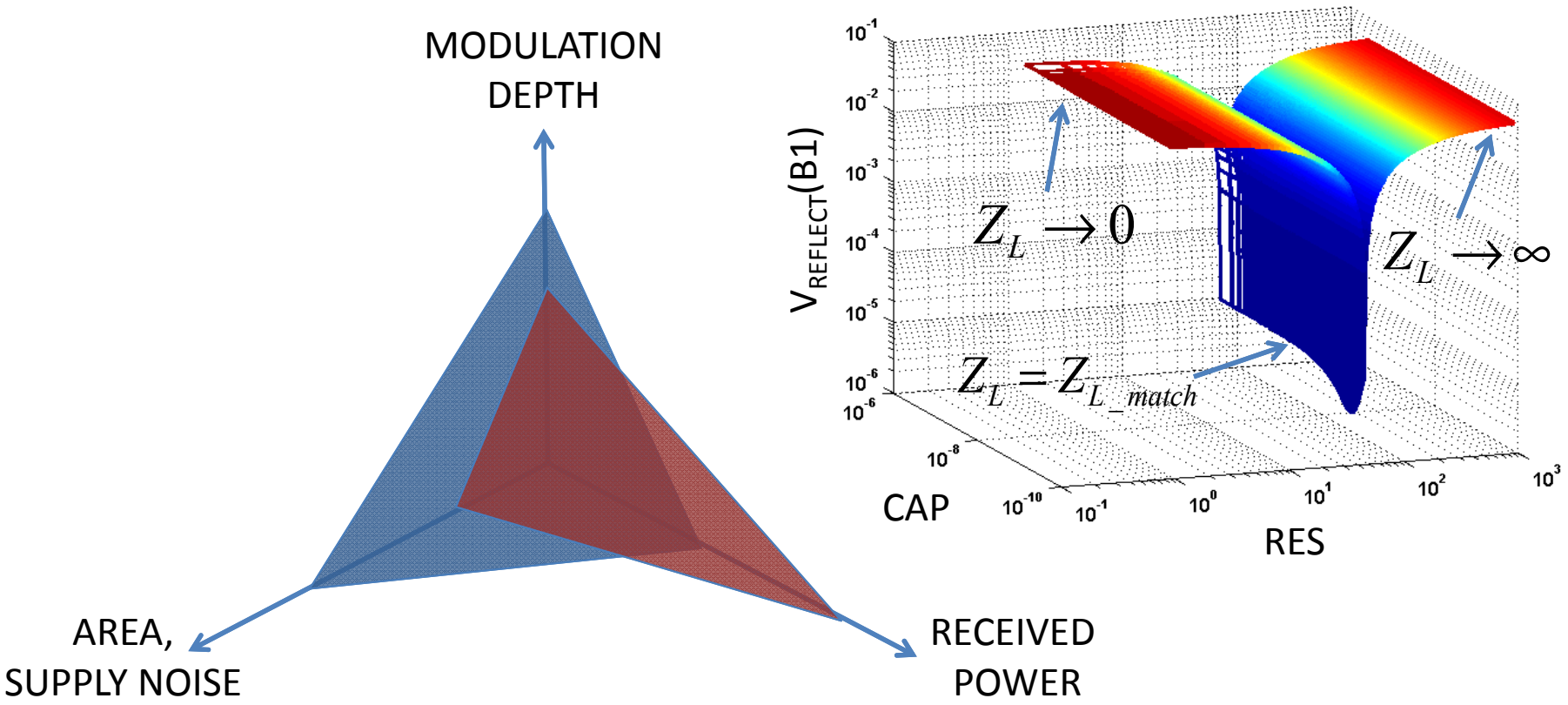
Wireless Data/Power Strategy





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Wireless Data/Power Strategy

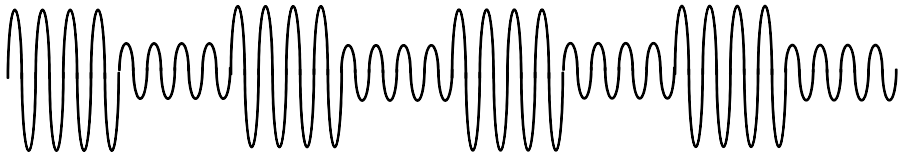


- Trade off modulation depth for simultaneous wireless data and power transfer
 - Reduce excessive wireless comm modulation depth

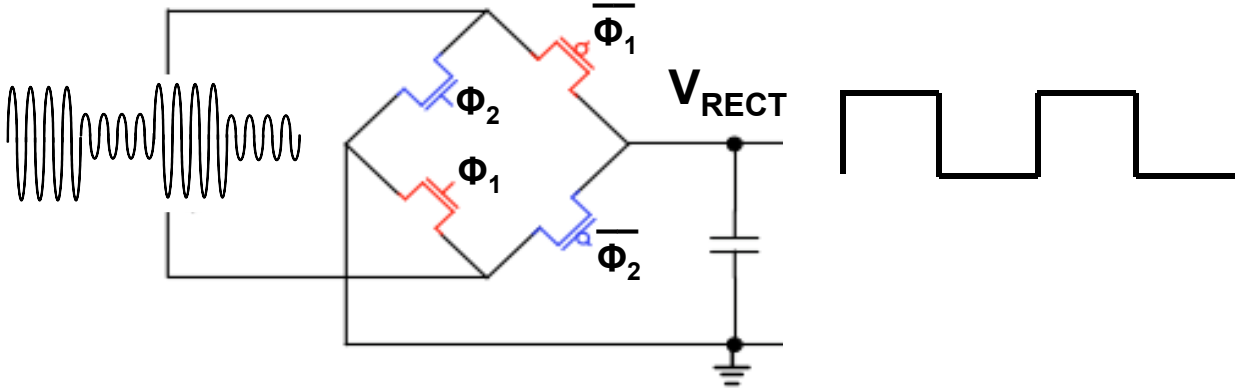
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Wireless Architecture

$V_{IN_P} - V_{IN_N}$

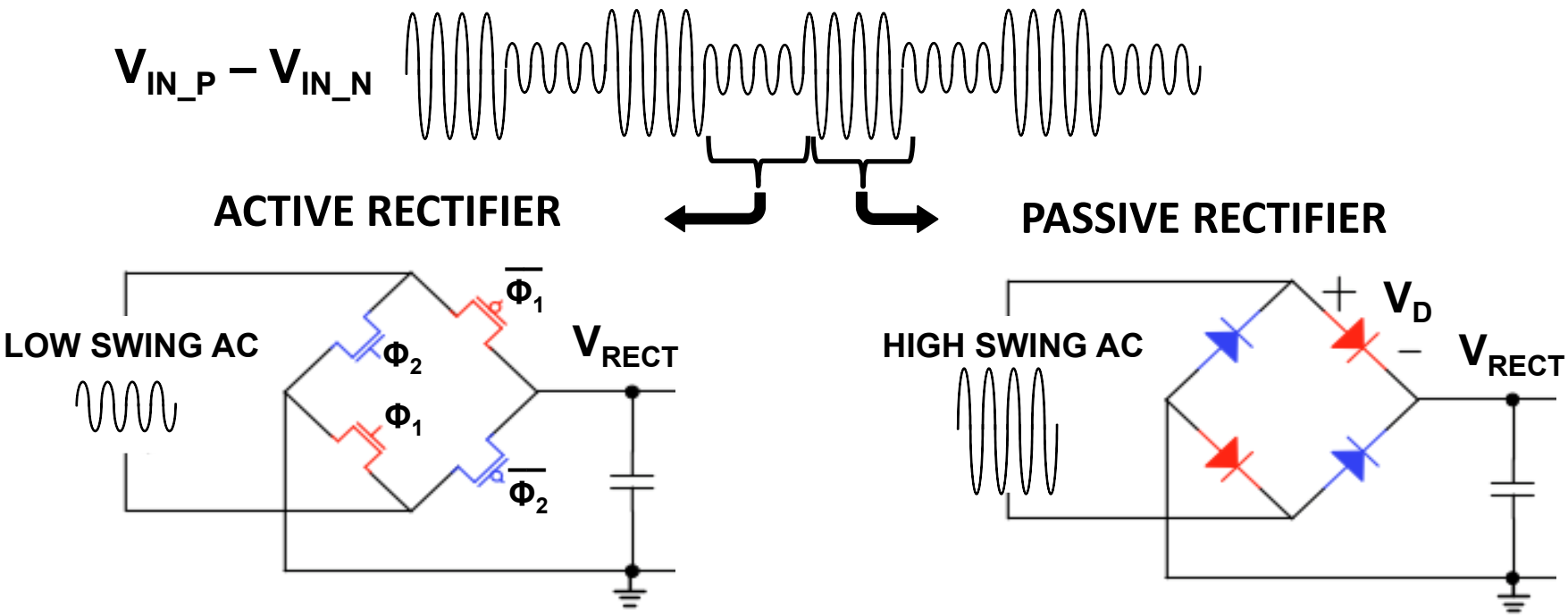


ACTIVE RECTIFIER



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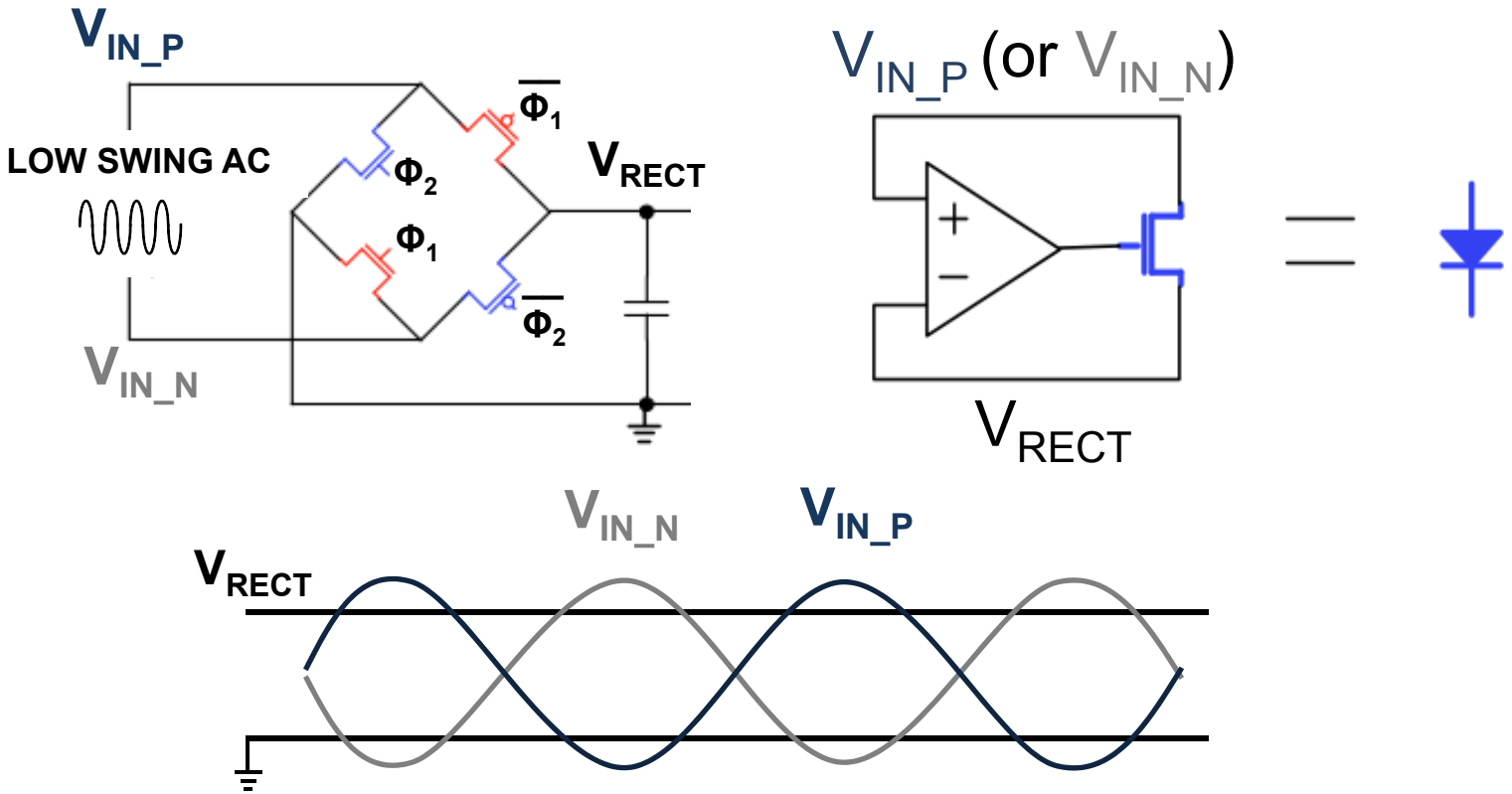
Wireless Architecture



- Dual rectifier smooths voltage ripple at V_{RECT}
 - Results in **decoupling capacitance 20x smaller**
 - Relaxes LDO specifications

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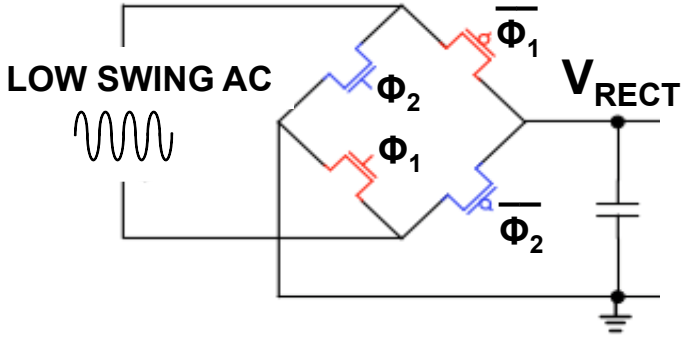
Conventional Active Rectifier

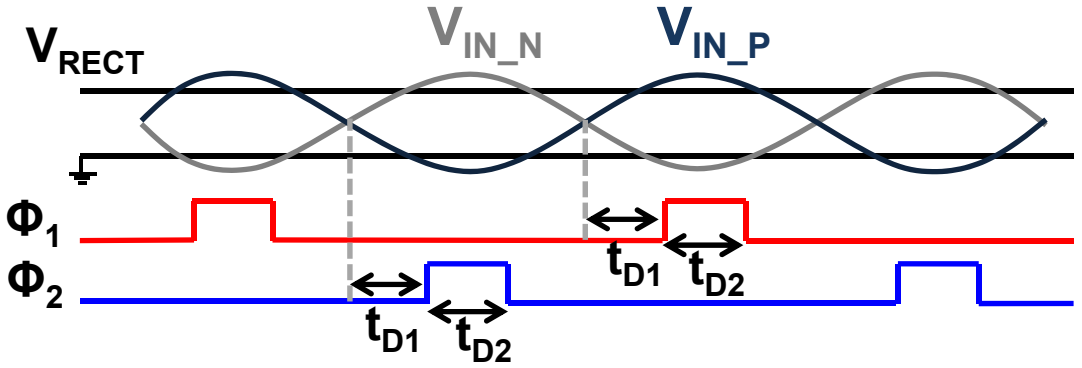


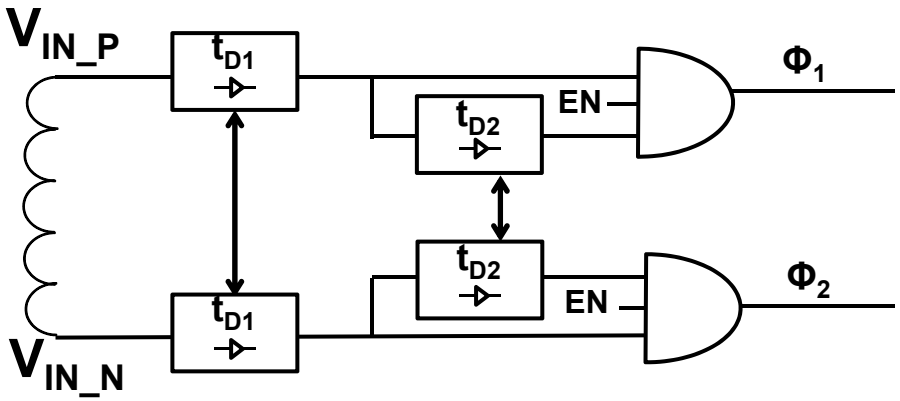
- Use comparator for synchronous rectification
 - Detect the points IN_P and IN_N cross V_{RECT}
- Need to operate at high frequency (300MHz)
 - High power (100s of μA), very inefficient

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Active Rectifier Implementation



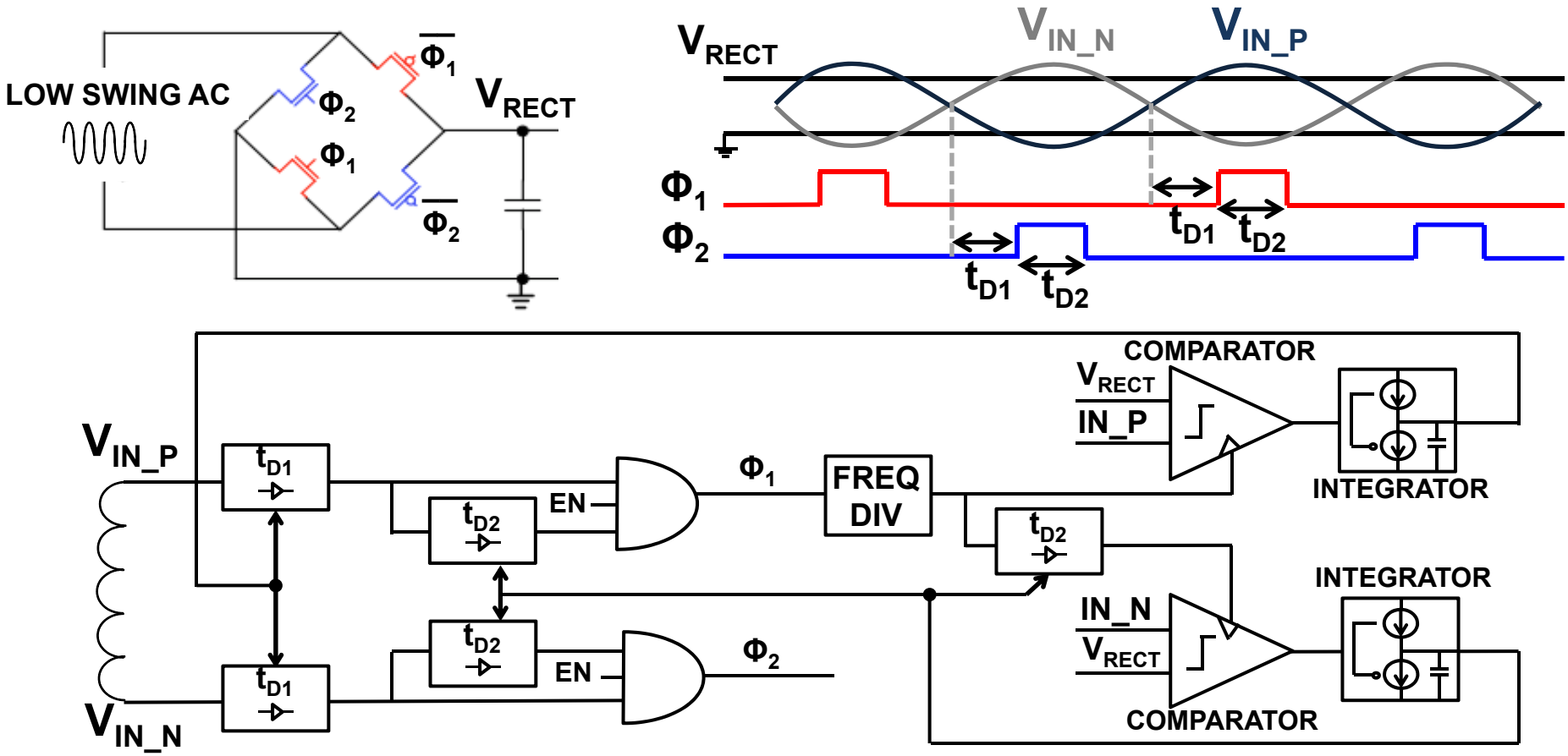




- Generate the gate signal from antenna terminal

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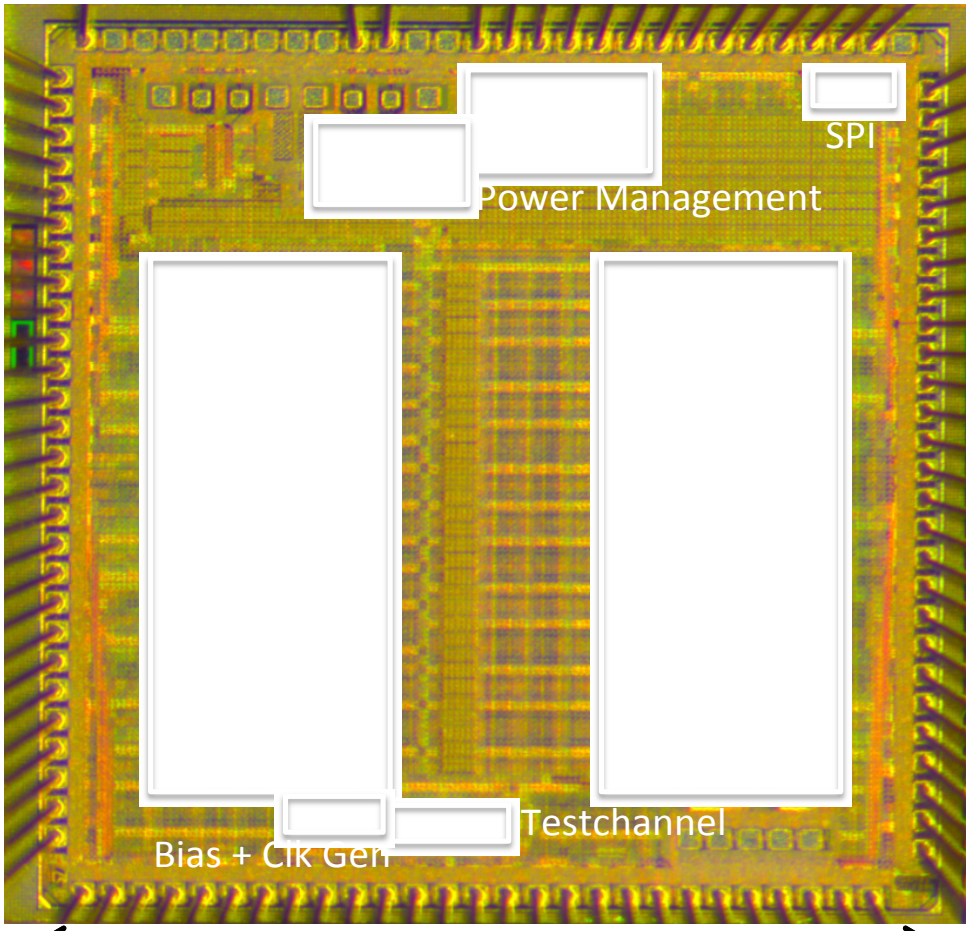
Active Rectifier Implementation



- Generate the gate signal from antenna terminal
- Use integral loops to tune timing (t_{D1}, t_{D2})
 - Comparators clocked at 38MHz to save power

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Measurement Results



65nm LPCMOS 1P7M

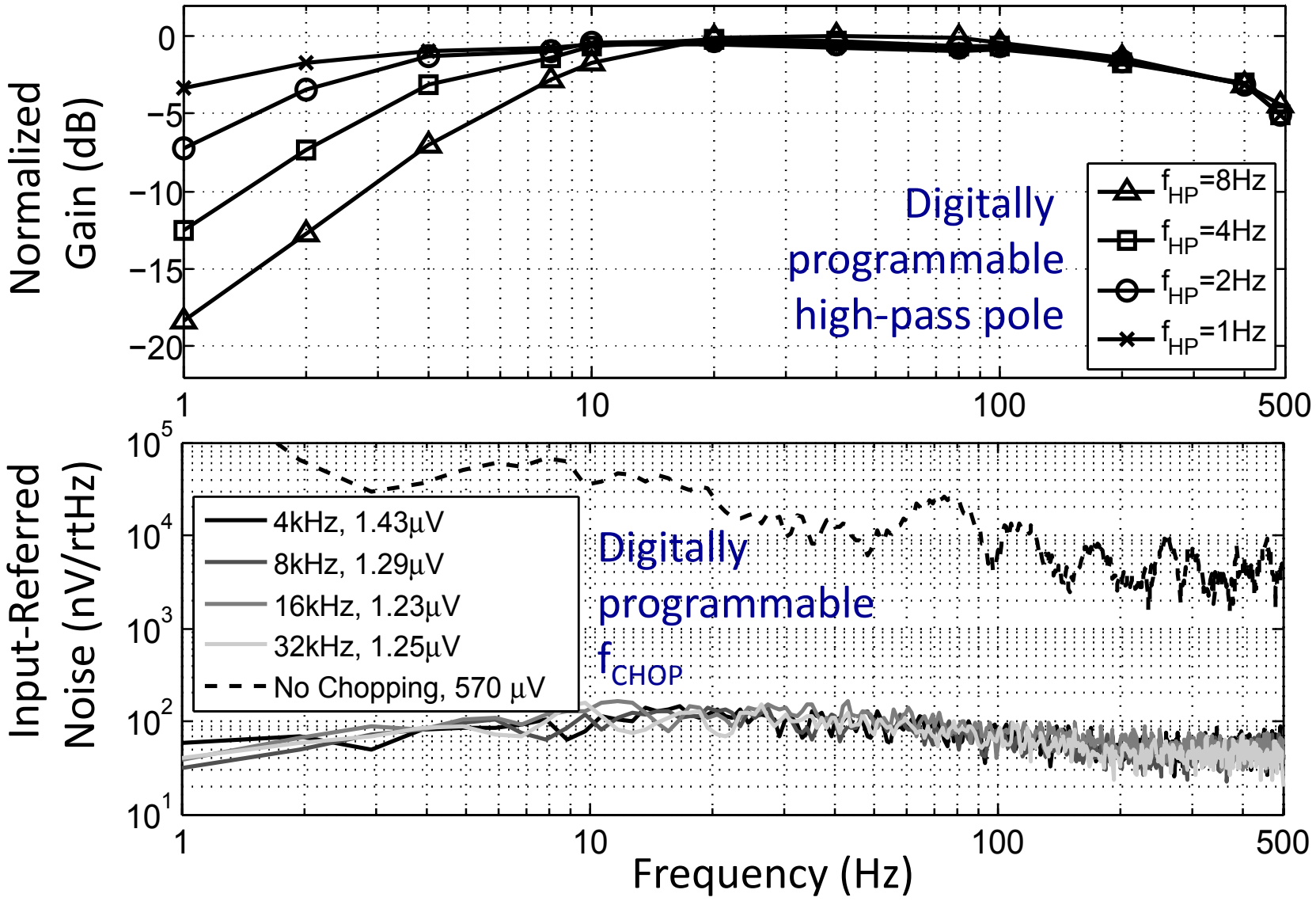
Requires only:

- Electrode/Antenna Array
- SPI Configuration

	Area (mm^2)	Power (µW)
64 FE ARRAY	1.6	147.2
TX & ENCODER	0.015	2.4
CLOCK RECOVERY	0.012	10.6
PMU	0.09	64.1
TOTAL	1.72	224.3

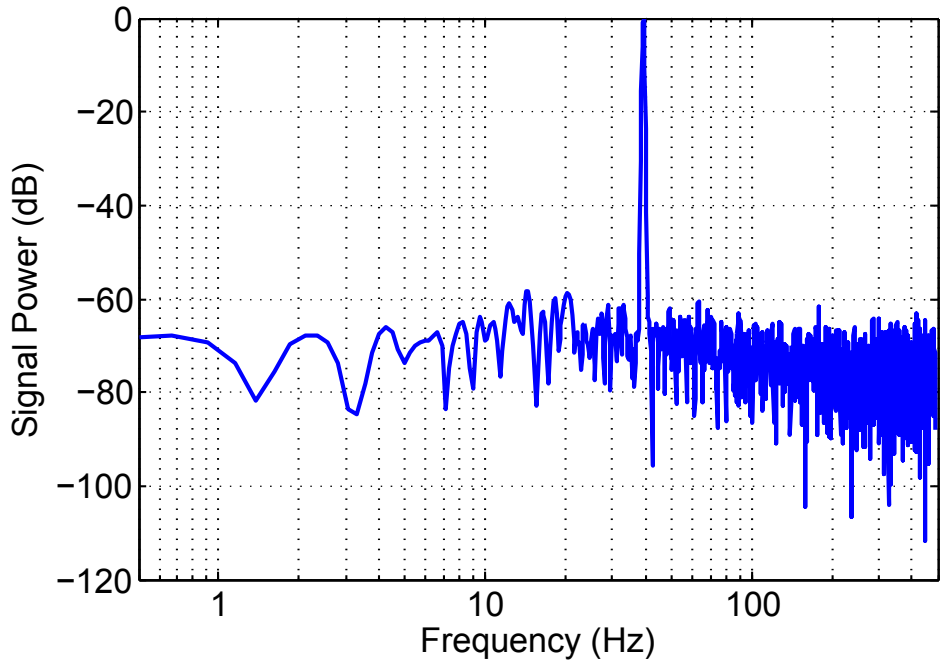
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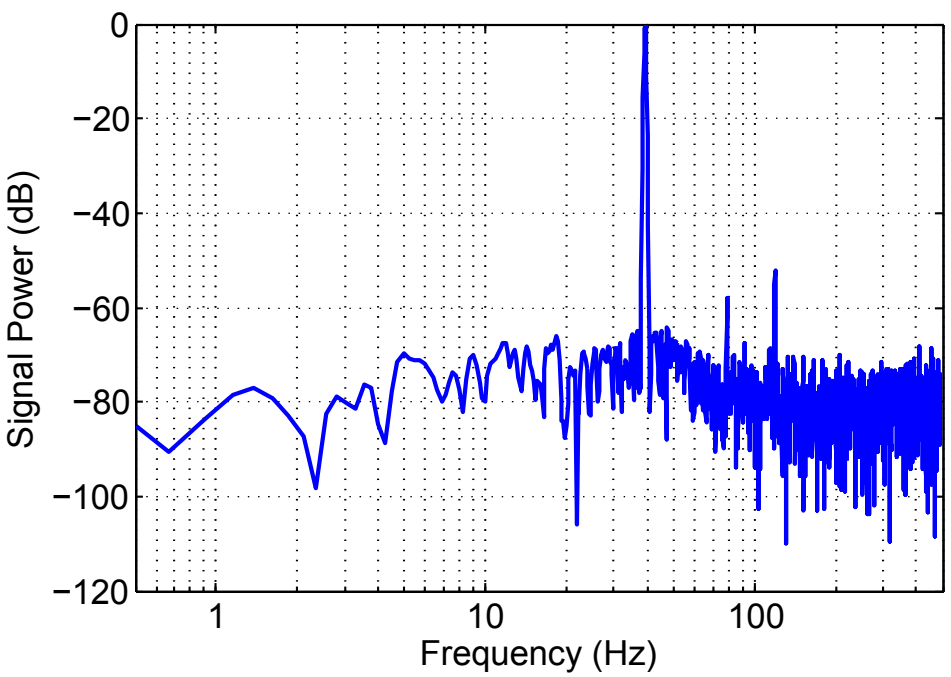
Front-end Measurements (I)



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Front-end Measurements (II)





0.5 mV_{ptp} input
>60dB SFDR
No visible harmonics

1.0 mV_{ptp} input
52dB SFDR
0.4% THD

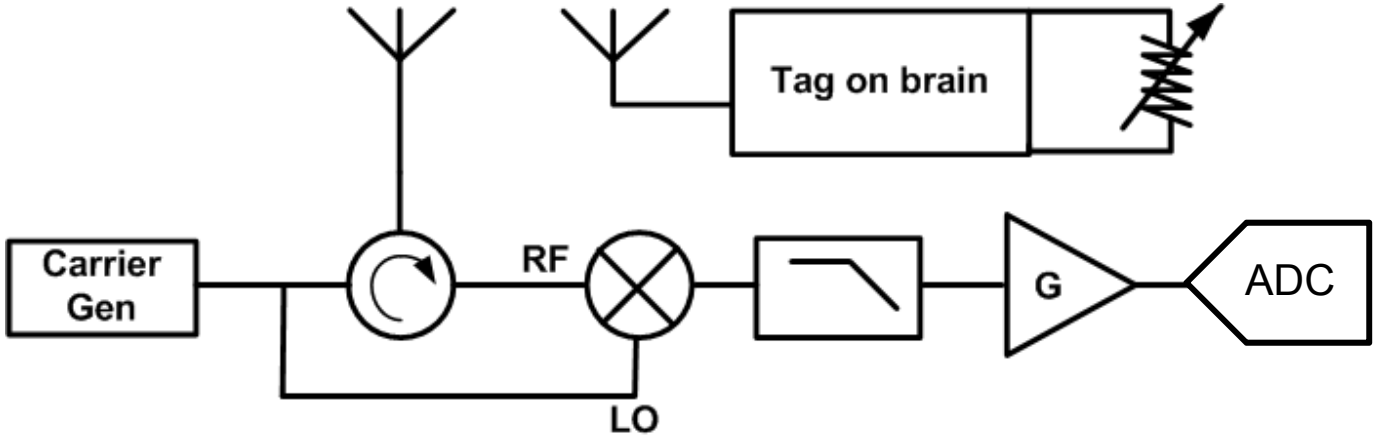
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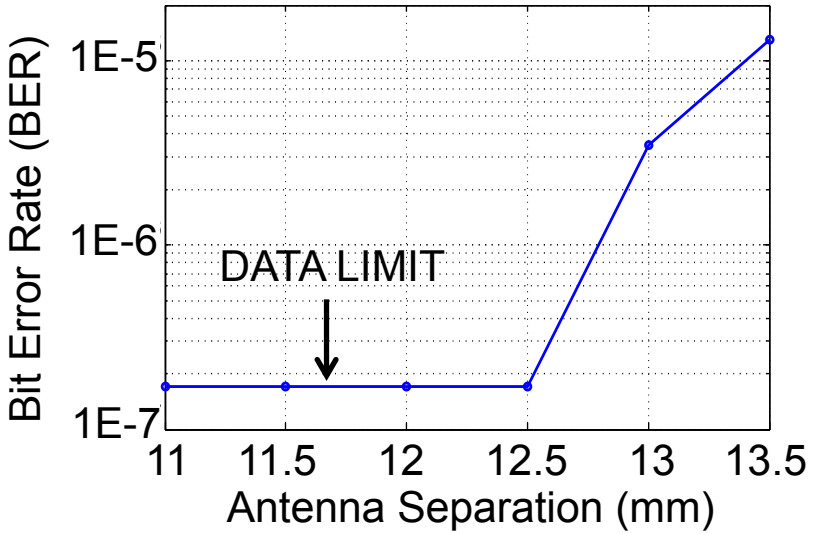
Front-end Comparison

*includes ADC **requires off-chip filter	Denison JSSC '07	Yacziglu JSSC '08	Zhang TCAS, '11	**Muller ISSCC '14**
V_{DD} (V)	1.8	3.0	1.2	**0.5**
Power (µW/ch)	2	33.3	3.24	**2.3***
IRNoise (nV/rtHz)	100	60	85	**58***
NEF (Noise x Current)	4.6	4.3	5.38	**4.76***
PEF (Noise x Power)	38.1	55.5	34.7	**11.3***
R_{IN} (MΩ)	8	1000	4	**28**
Max Input Offset (mV)	+/-50mV	45mV	0mV**	**+/-50mV**
CMRR/PSRR (dB)	100/--	120/--	80/60	**88/67***
Area (mm^2/ch)	0.8	0.5	0.4	**0.025***
ADC Resolution	none	11-bit	none	**15-bit**
# of Channels	1	8	1	**64**
Technology	0.8µm	0.5µm	0.13µm	**65nm**

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Wireless Data Measurements



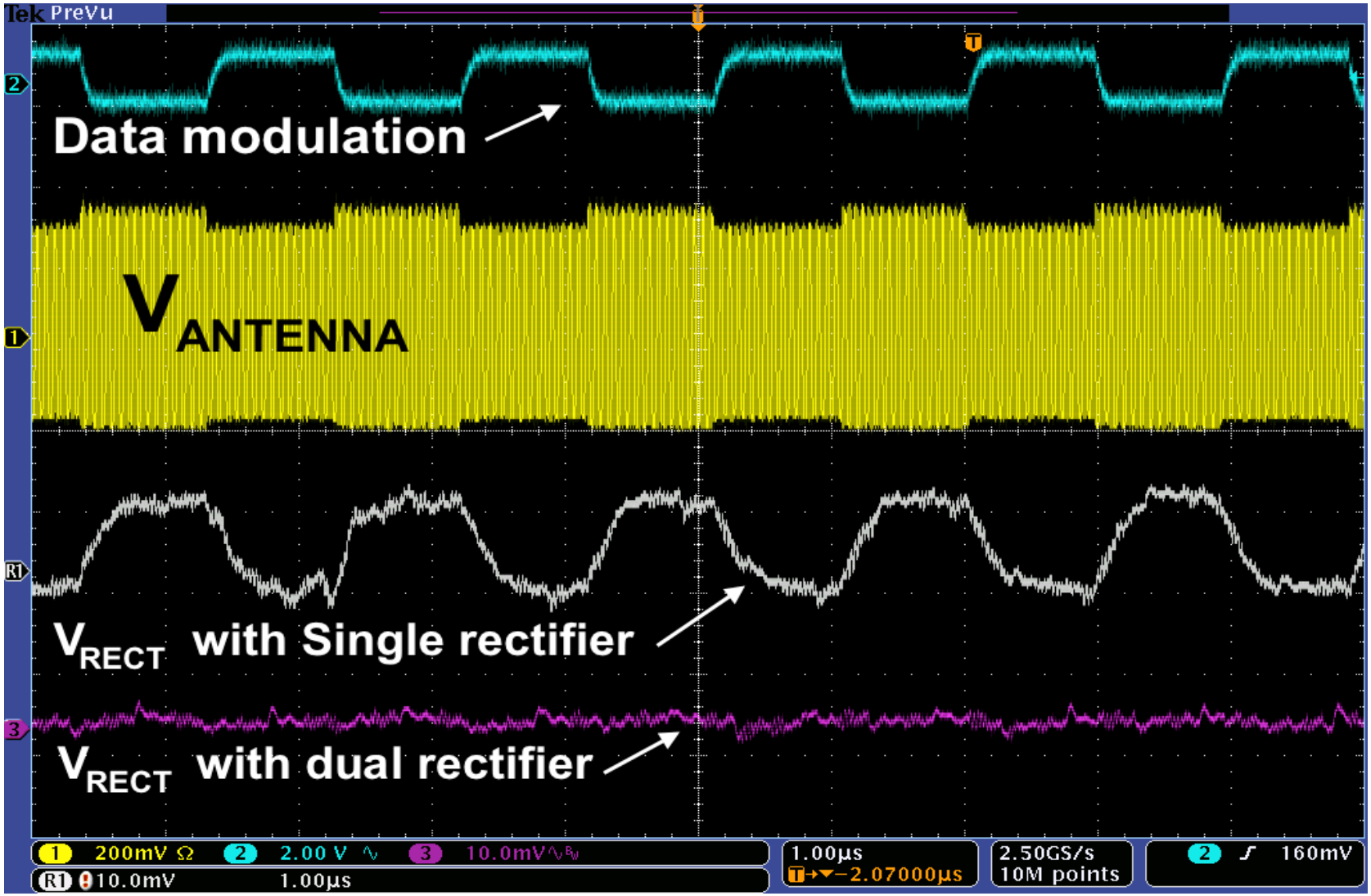


	Tx & Encoder	Clock Recovery
Power	2.4µW	10.6µW
Data-rate	1Mbps	--
FOM	2.4pJ/bit	--
BER	< 1.7E-7	**--**

- Transmitted PRBS-7 data air and *in vivo*
 - Zero errors in 5.9Mb at 10mm distance

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Wireless Power and Data



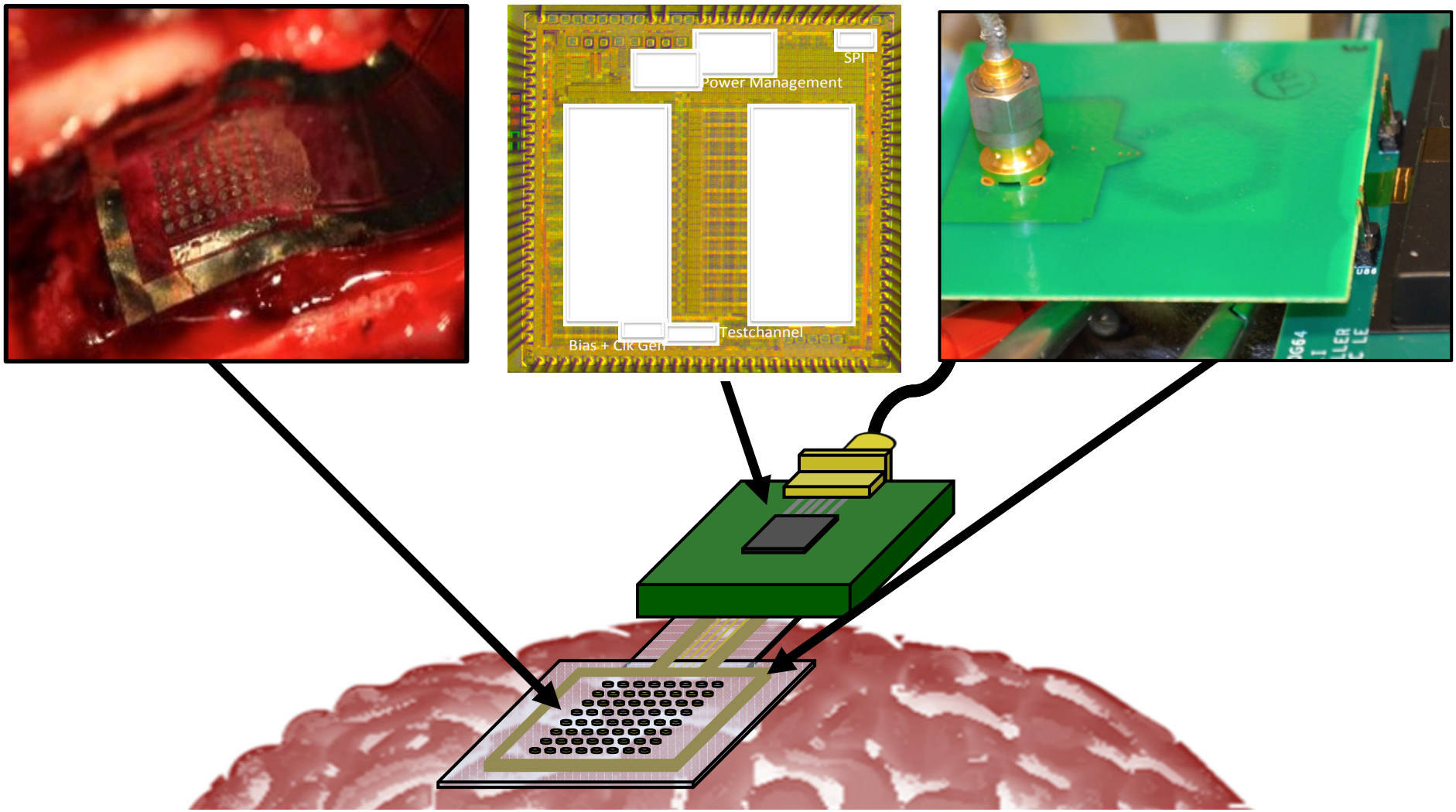
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In Vivo Measurement Setup

ELECTRODES

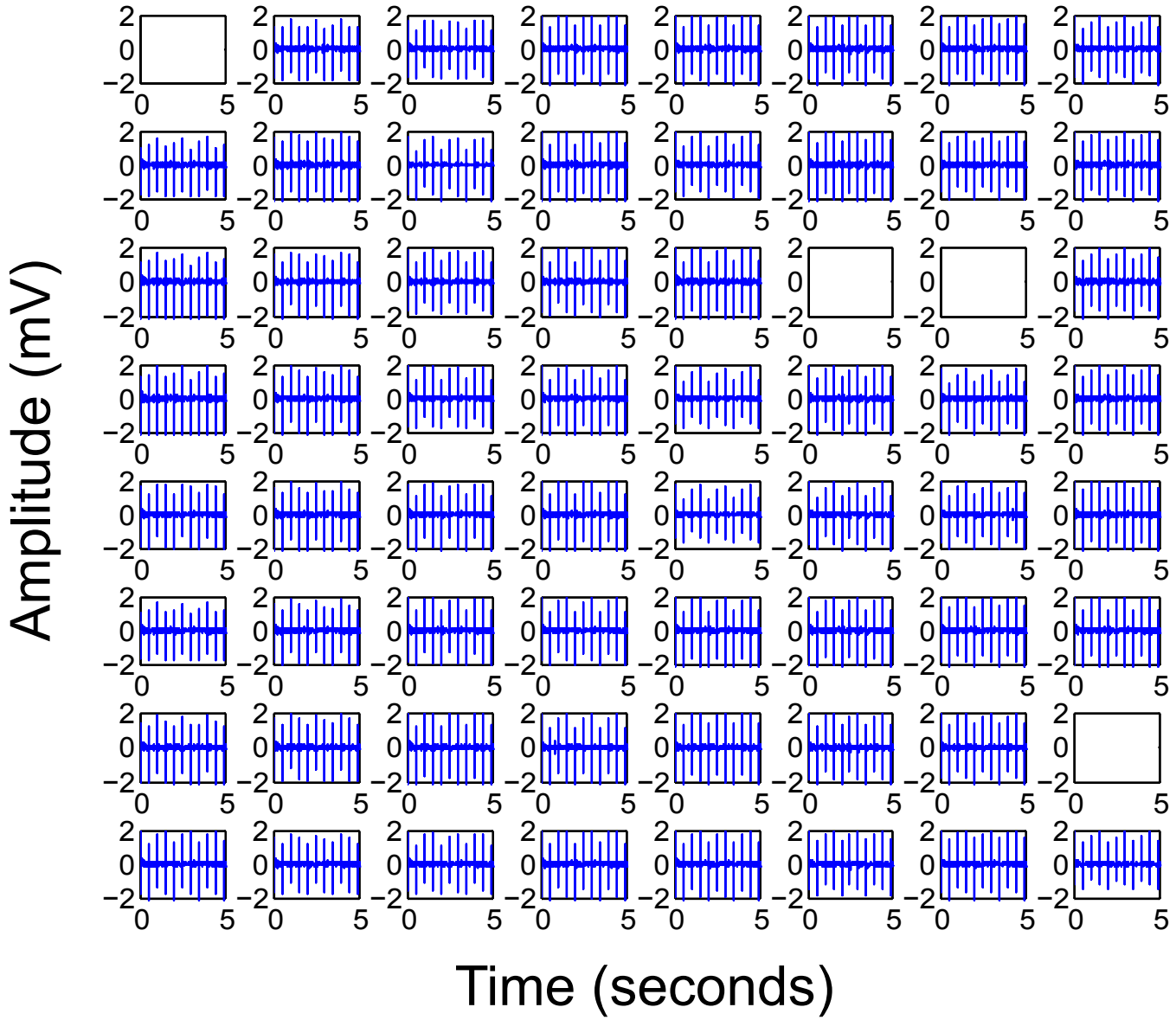
ASIC

ANTENNAS



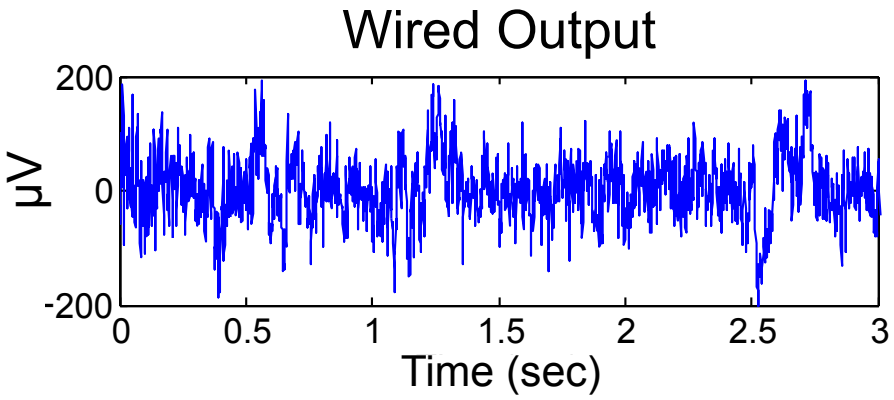
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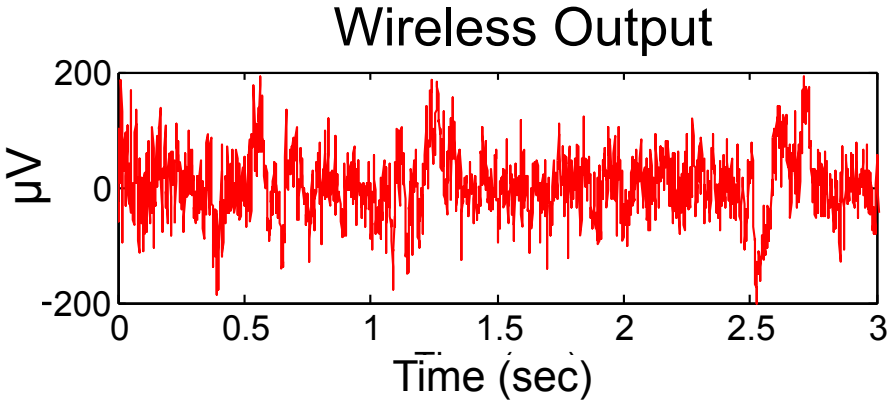
In vivo Measurements (I)



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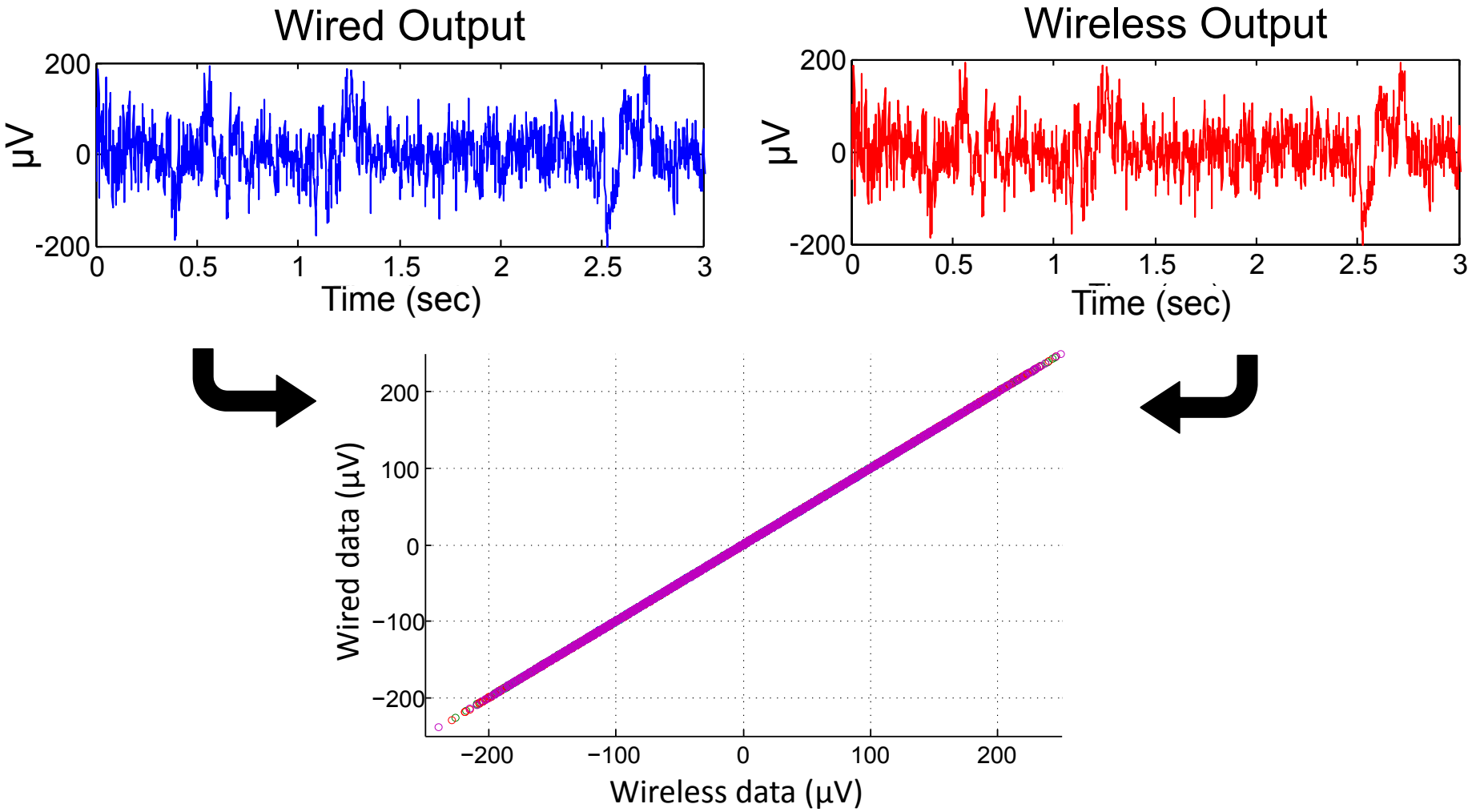
In vivo Measurements (II)





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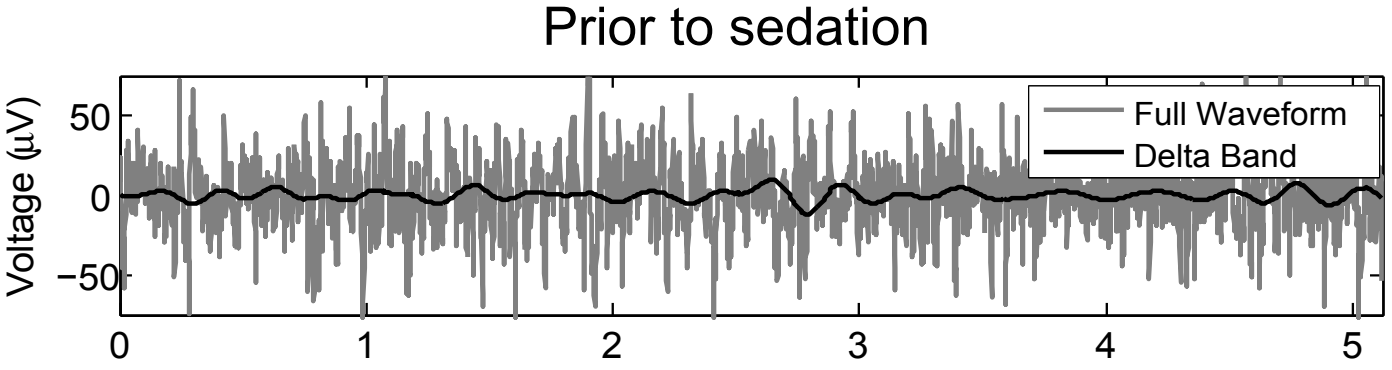
In vivo Measurements (II)

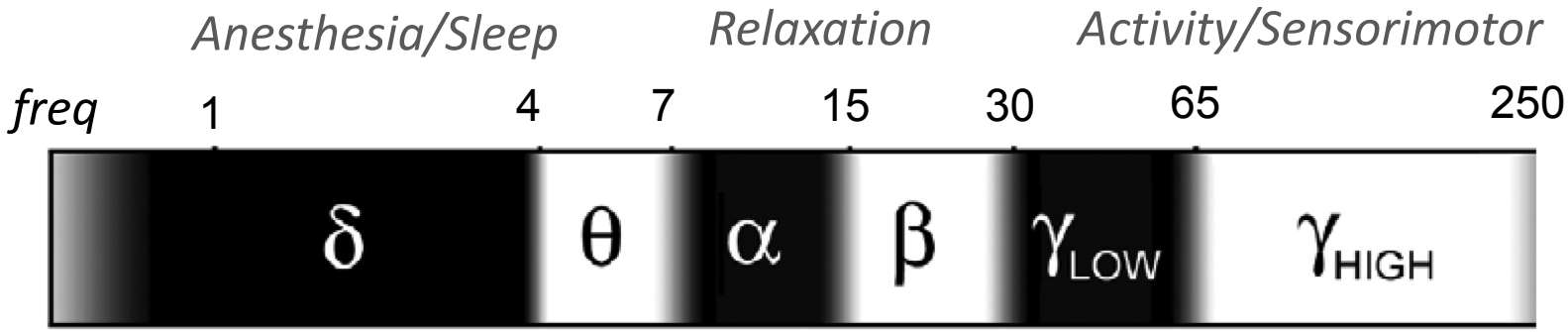


- Scatterplot of wired and wireless outputs
 - Zero errors in > 3Mb of data

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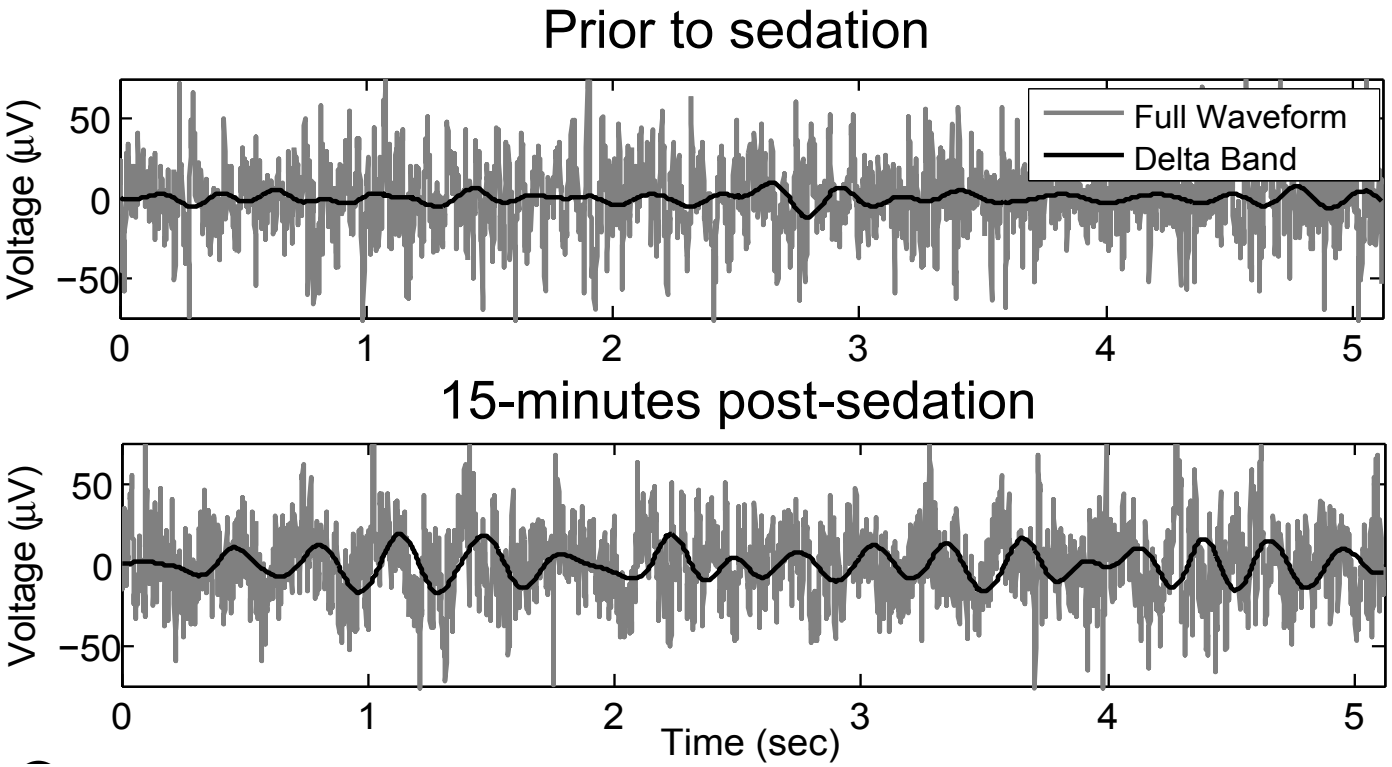
In vivo Measurements (III)

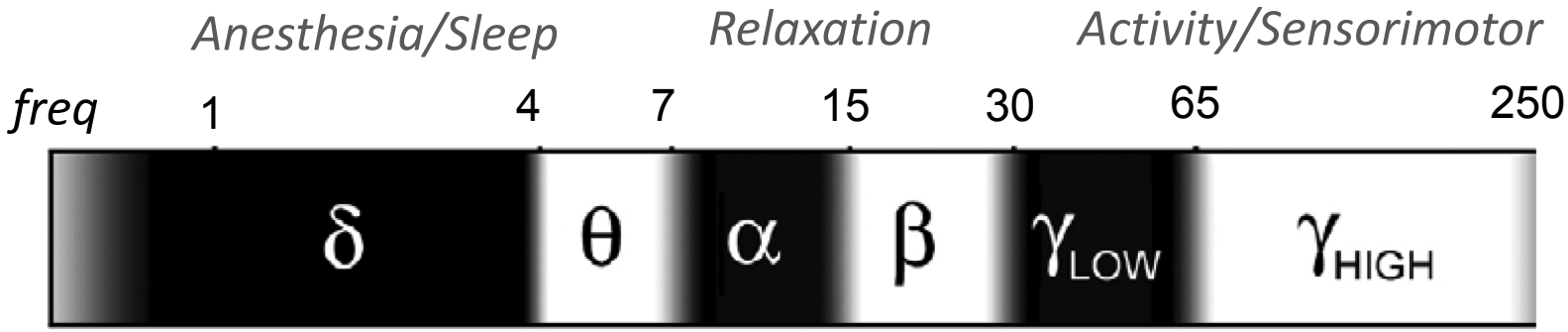




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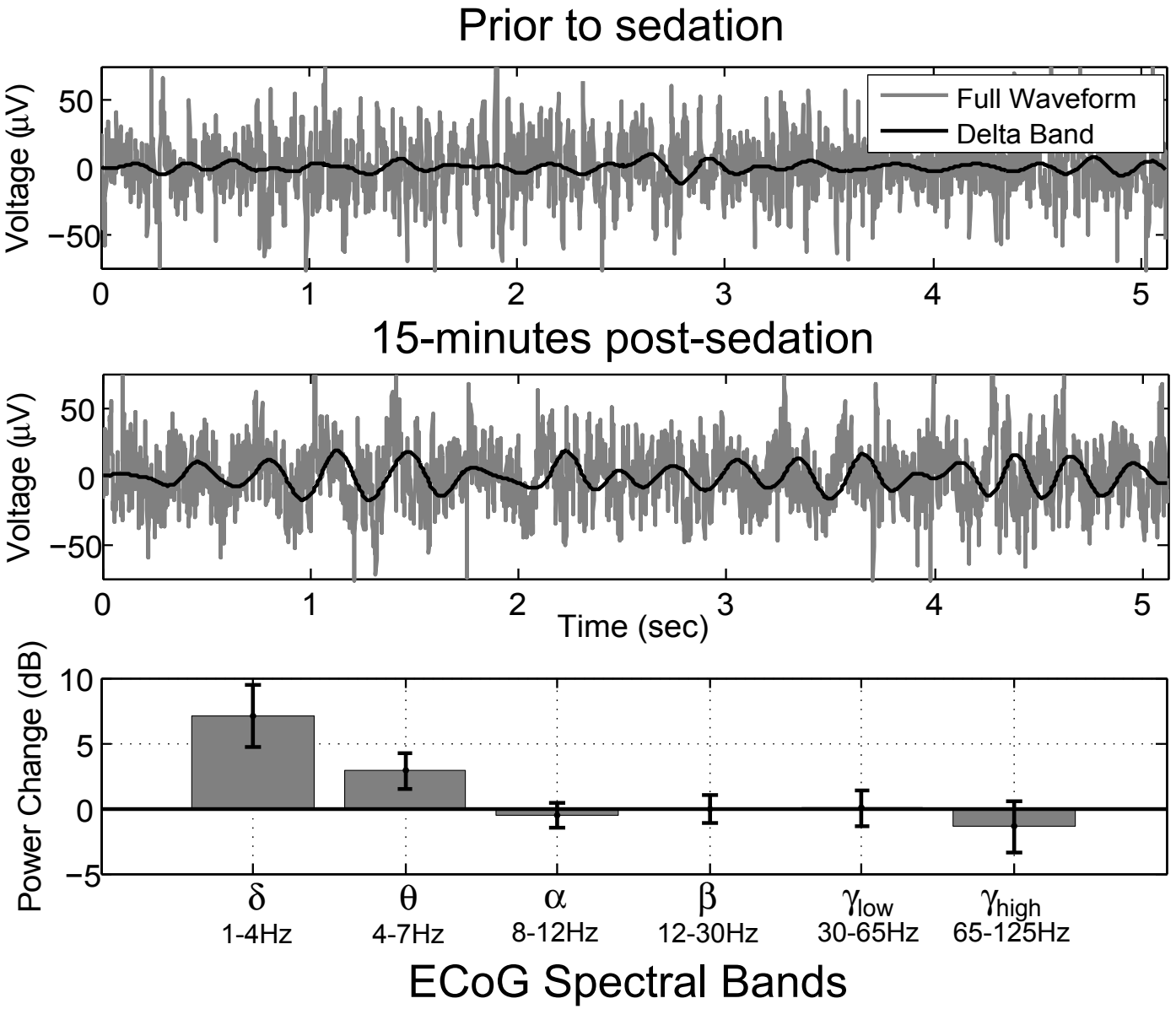
In vivo Measurements (III)





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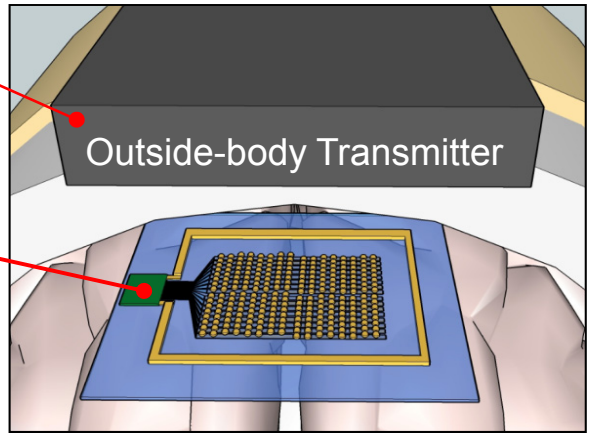
In vivo Measurements (III)



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Summary

- 64-channel wireless ECoG neural sensor
- **SAFE** power levels
 - Operation **3x lower power** than IEEE/FCC recommendation
- Extremely small size
 - Over **16x decrease in die area**
 - No external capacitors



- *Excellent prospect to become the technology of choice for clinically-relevant neural recording*

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Acknowledgments

- ST Microelectronics for chip fabrication
- BDA for Analog FastSpice
- Students, staff and sponsors of the Berkeley Wireless Research Center (BWRC) and the Multi-Scale Systems Center (MuSyC)
- Center for Neural Engineering and Prosthesis
- Filip Maksimovic, Lingkai Kong, Nathan Narevsky, Lu Ye

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A Power-Efficient Switched-Capacitor Stimulating System for Electrical/Optical Deep-Brain Stimulation

Hyung-Min Lee[1], Ki-Yong Kwon[2], Wen Li[2], and Maysam Ghovanloo[1]

GT-Bionics Lab
www.GTBionics.org

[1]Georgia Institute of Technology, Atlanta, GA
[2]Michigan State University, East Lansing, MI





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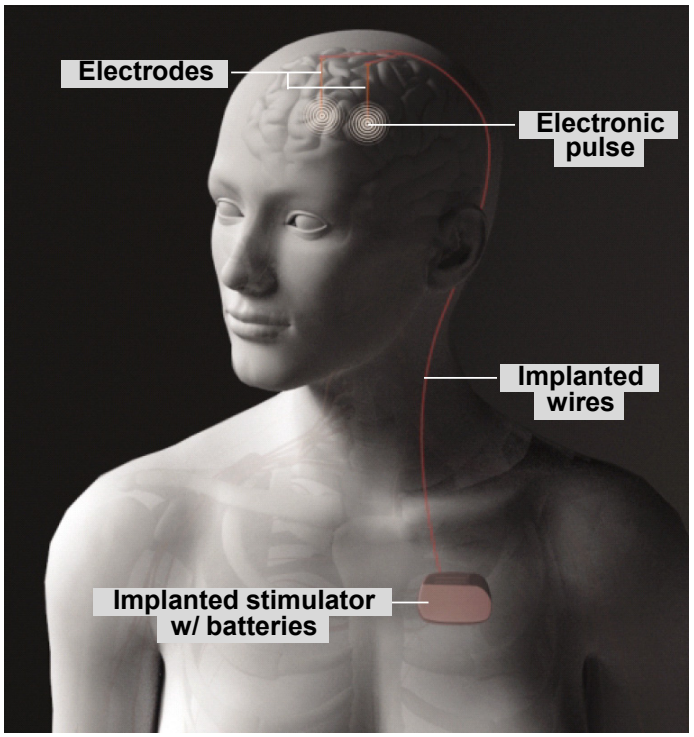
Neural Stimulating IMD Applications



Boston Retinal Prosthesis



Nucleus Cochlear Implant



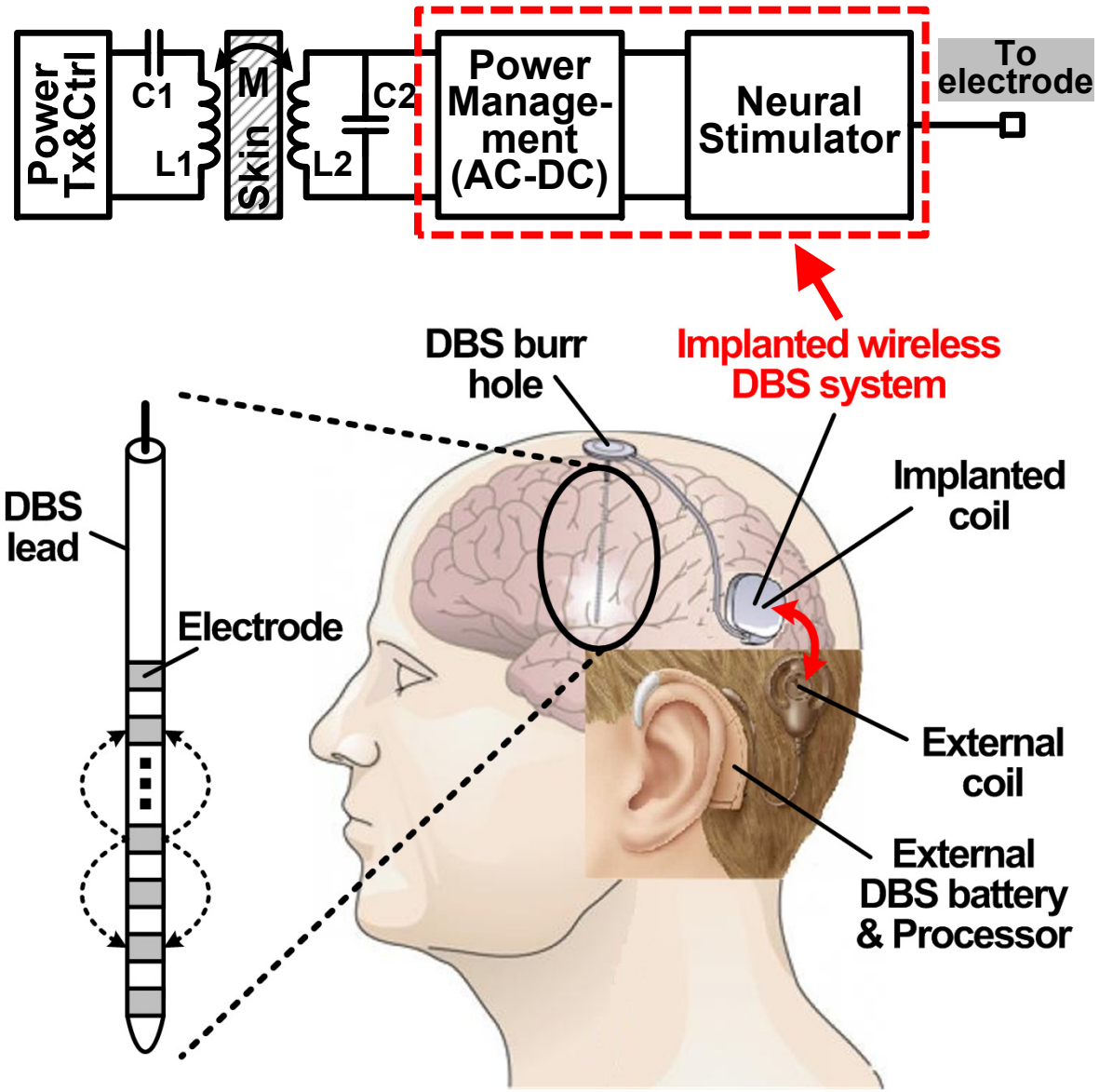
Chest-mounted Deep Brain Stimulation (DBS)

- Alleviate neurological diseases (DBS) or substitute sensory modalities (retinal/cochlear implant), high power, large volume
- Battery-powered chest-mounted DBS

 → Head-mounted DBS with wireless power transfer

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Wireless Neural Stimulating System



[Head-mounted Inductively-powered DBS system]

- A head-mounted DBS w/ inductive power from external energy source
- High power efficiency & safety are required for effective stimulation

Switched-capacitor based stimulation (SCS)

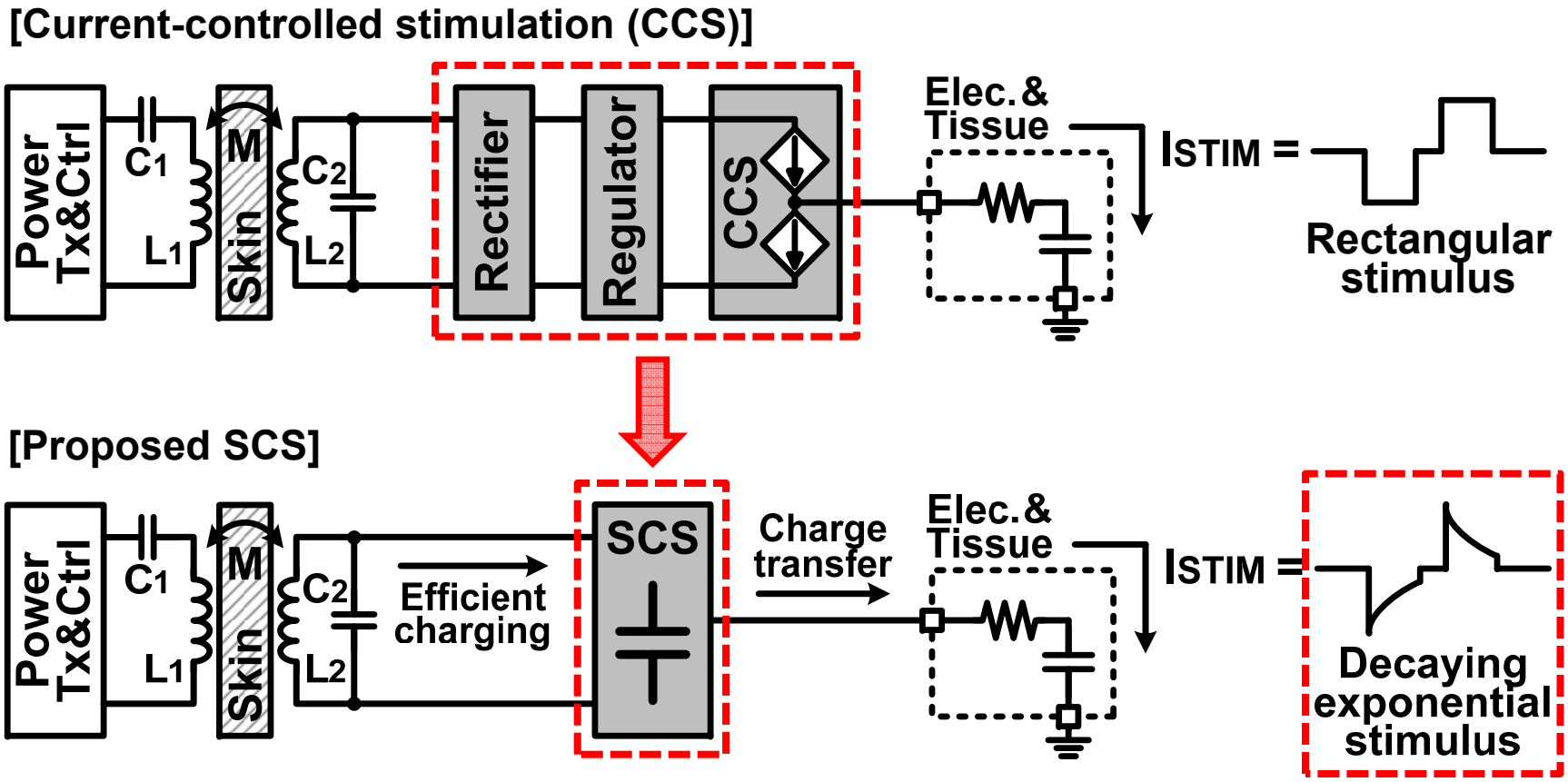
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Outline

- Switched-Capacitor Stimulation (SCS) Concept
- Power-Efficient SCS System
 - System architecture
 - Circuit details and implementation
 - Measurement results
- Energy-Efficient Stimulus Waveform
- Animal Experiments with SCS
 - *In vivo* electrical stimulation
 - *In vivo* wireless optogenetics
- Conclusions

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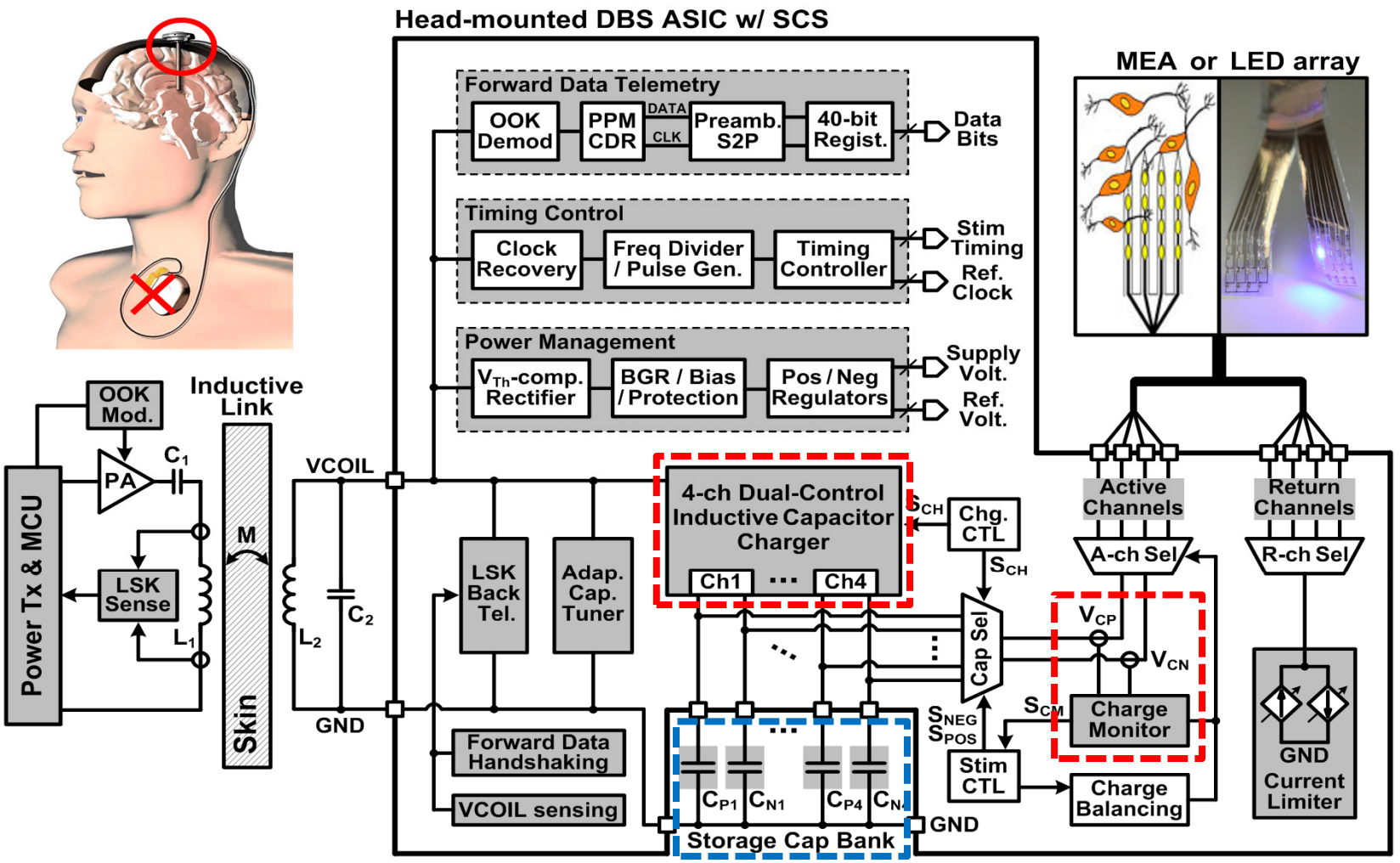
Switched-Capacitor Stimulation (SCS)



- Efficient capacitor charging → High stimulator efficiency
- Precise charge transfer → Safe charge-based stimulation
- Decaying-exponential waveform → High stimulus efficacy

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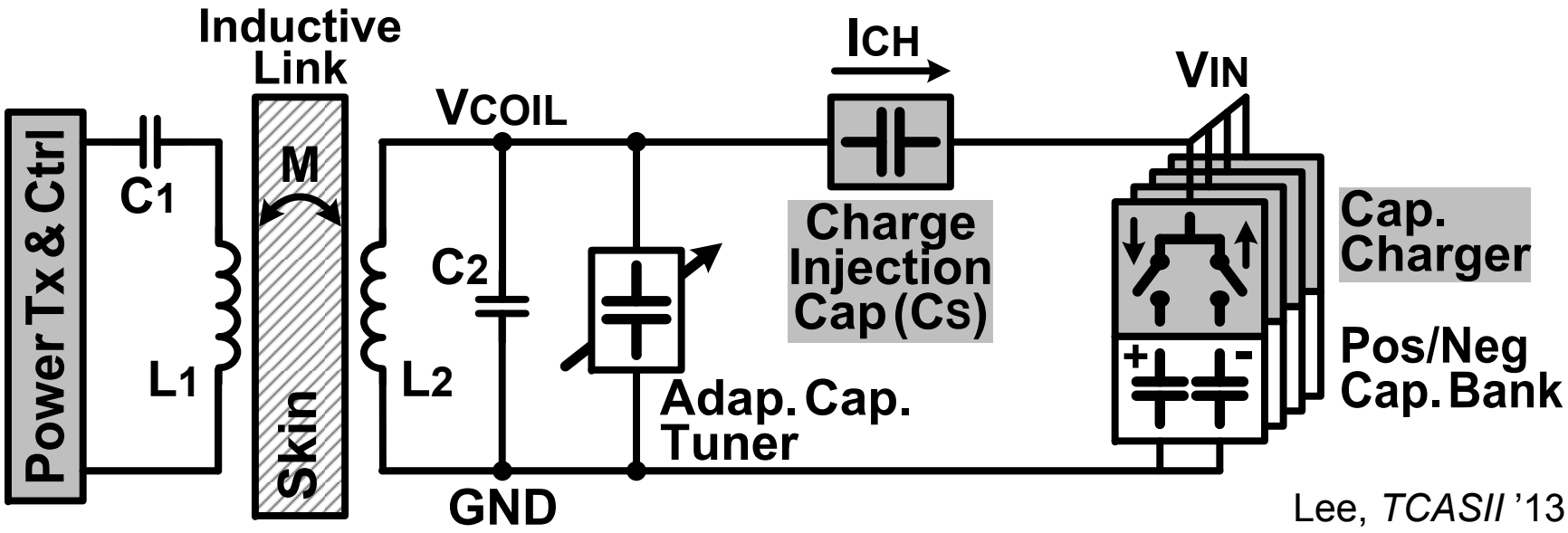
Power-Efficient SCS System Architecture



- Capacitor bank charging directly from an inductive link
- Charge monitoring for balanced charge transfer to MEA or LED

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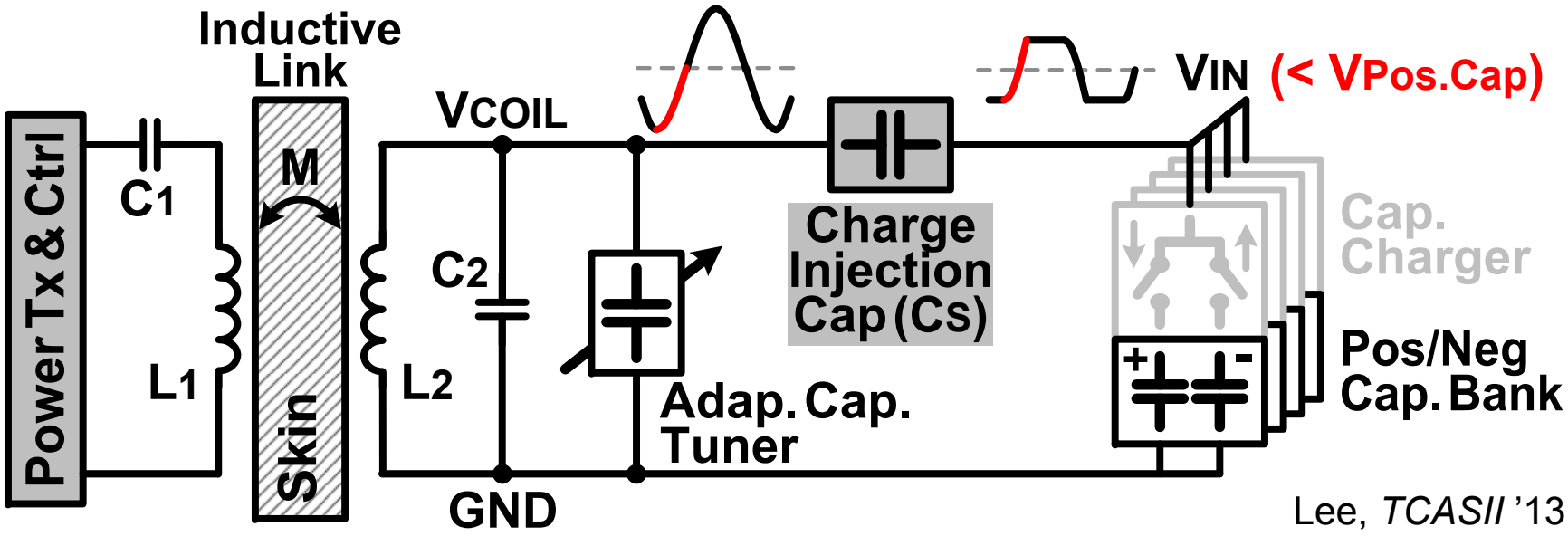
Inductive Capacitor Charging



- Direct pos/neg capacitor charging from AC coil voltage (V_{COIL})
- A charge injection capacitor (C_S) & a capacitor charger generate the fixed amount of charging current (I_{CH}).
- Fixed I_{CH} reduces switching loss, while C_S does not dissipate power, maximizing capacitor charging efficiency.

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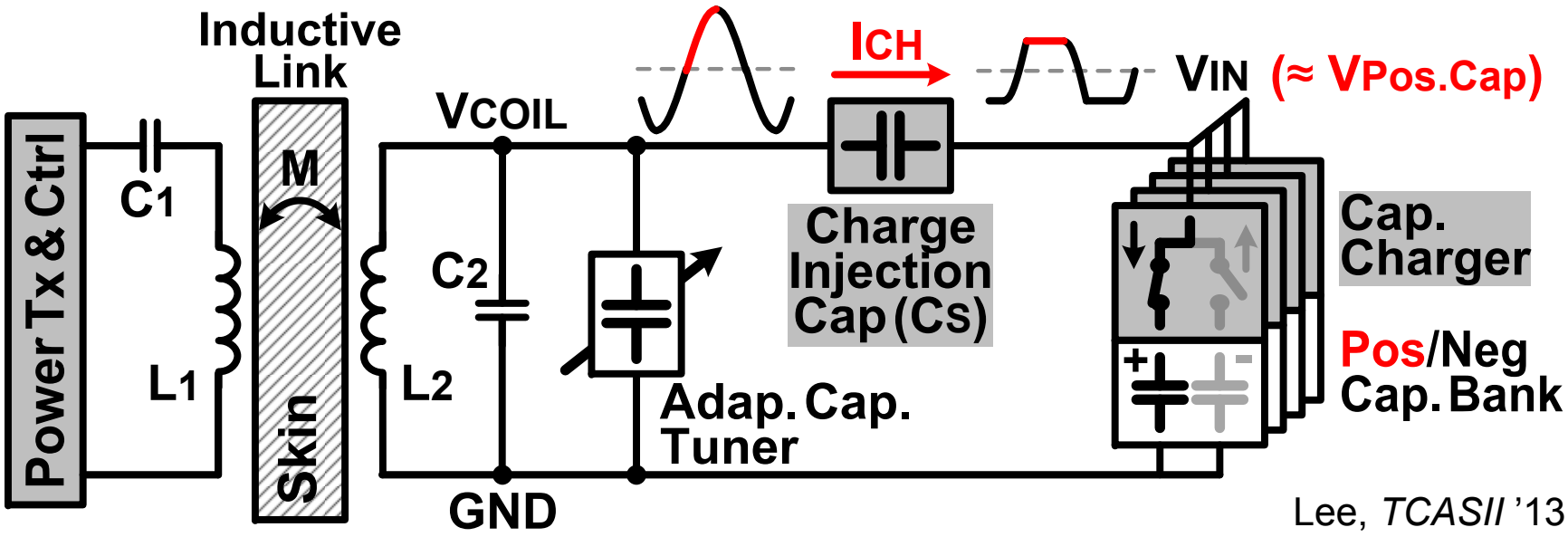
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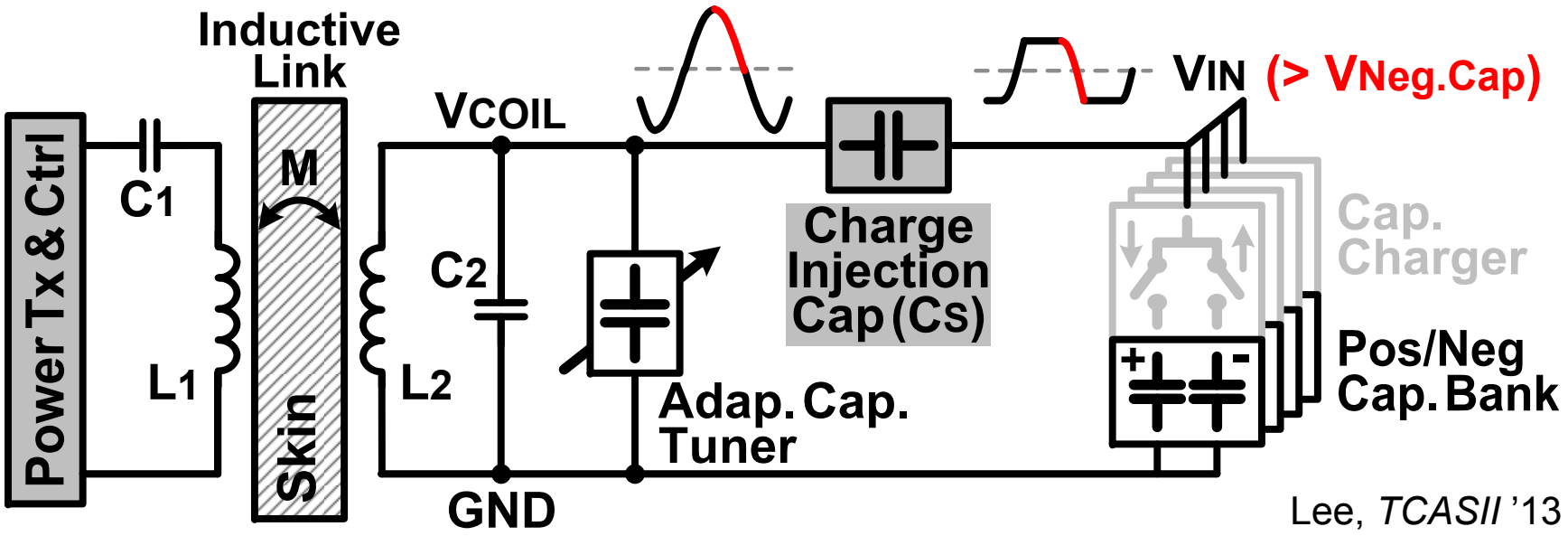
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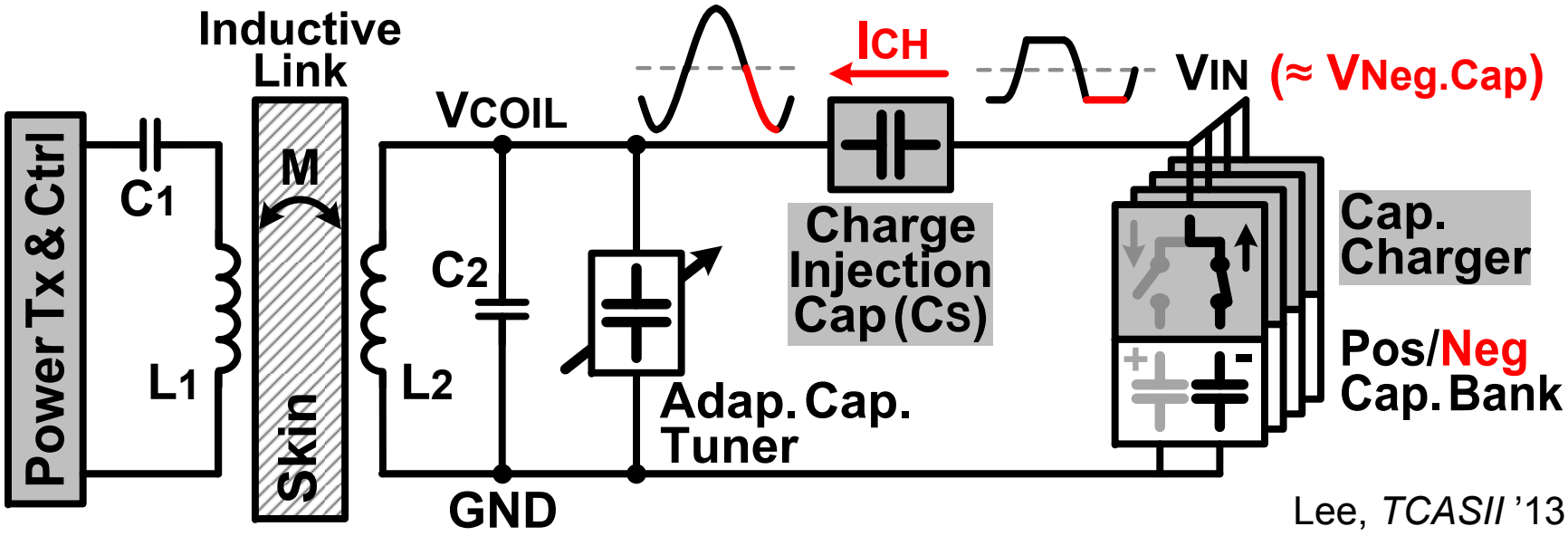
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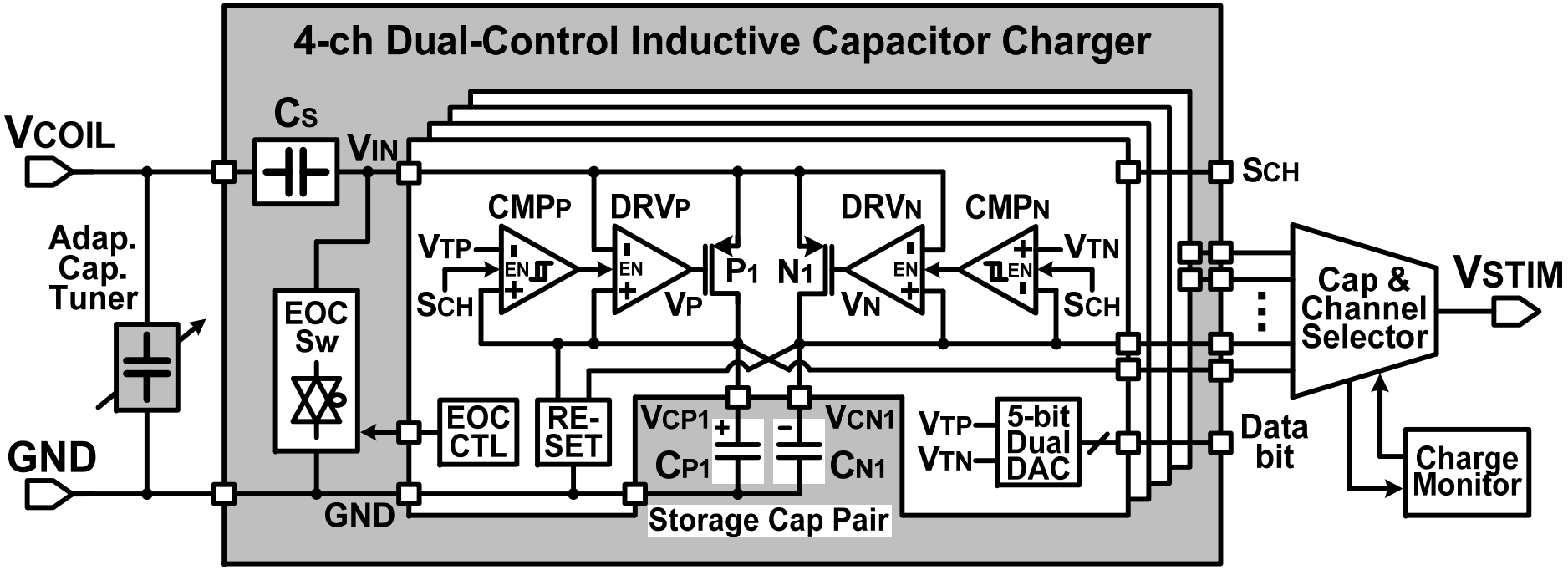
Inductive Capacitor Charging



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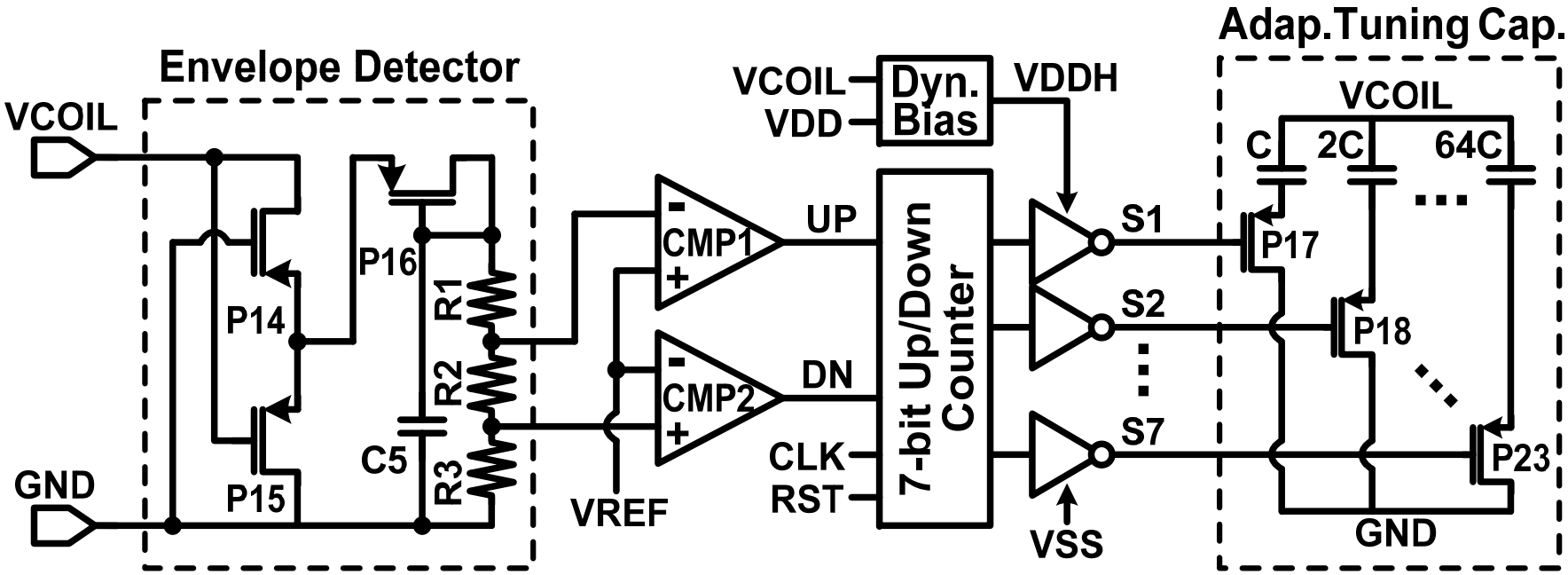
Dual-Control Inductive Capacitor Charger



- Dual-voltage control capability for separately charging pos/neg capacitors to each target voltage
- Capacitor reset function
- Adaptive capacitor tuning

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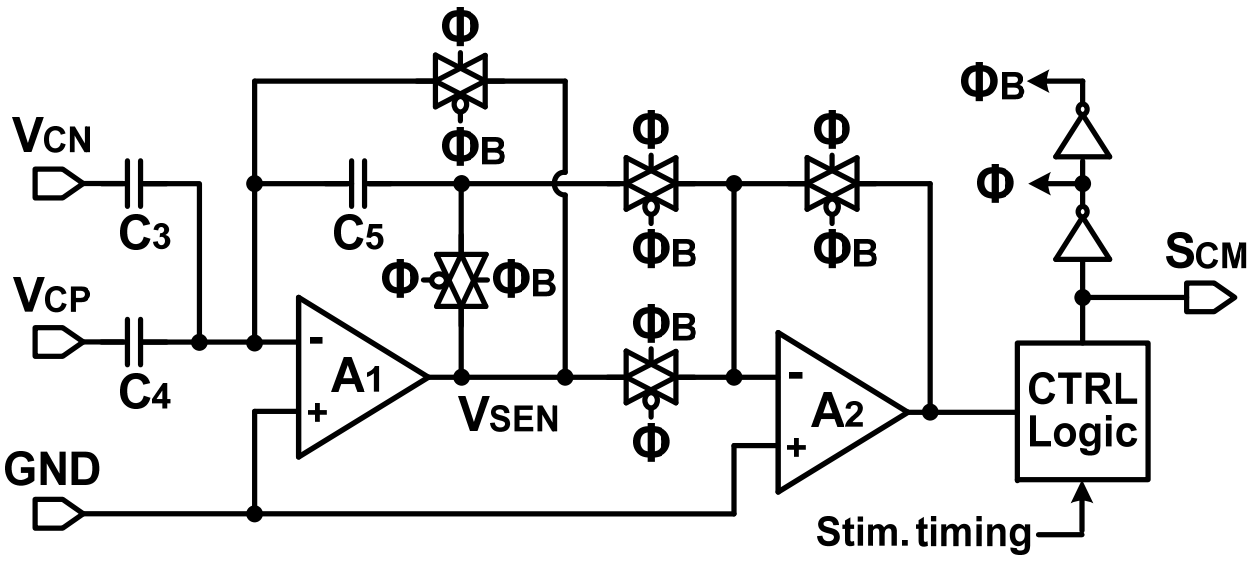
Adaptive Resonant Capacitor Tuner

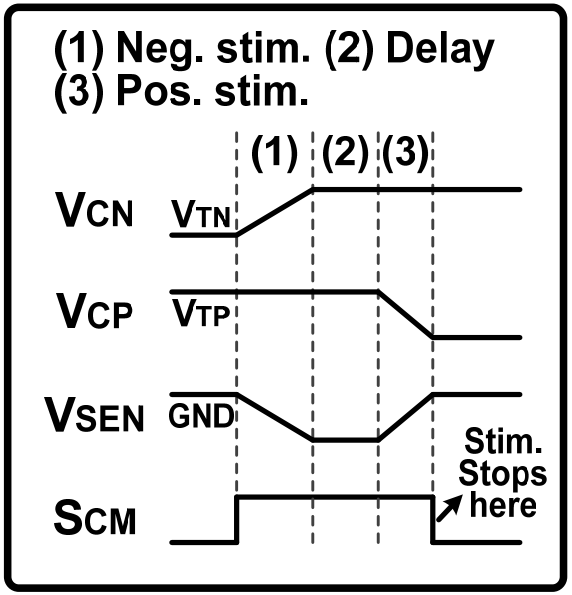


- Effective resonance capacitance varies during charging.
- Coil amplitude detection & comparison
- Adaptive 7-bit tuning capacitors

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Charge Monitoring (CM) Circuit

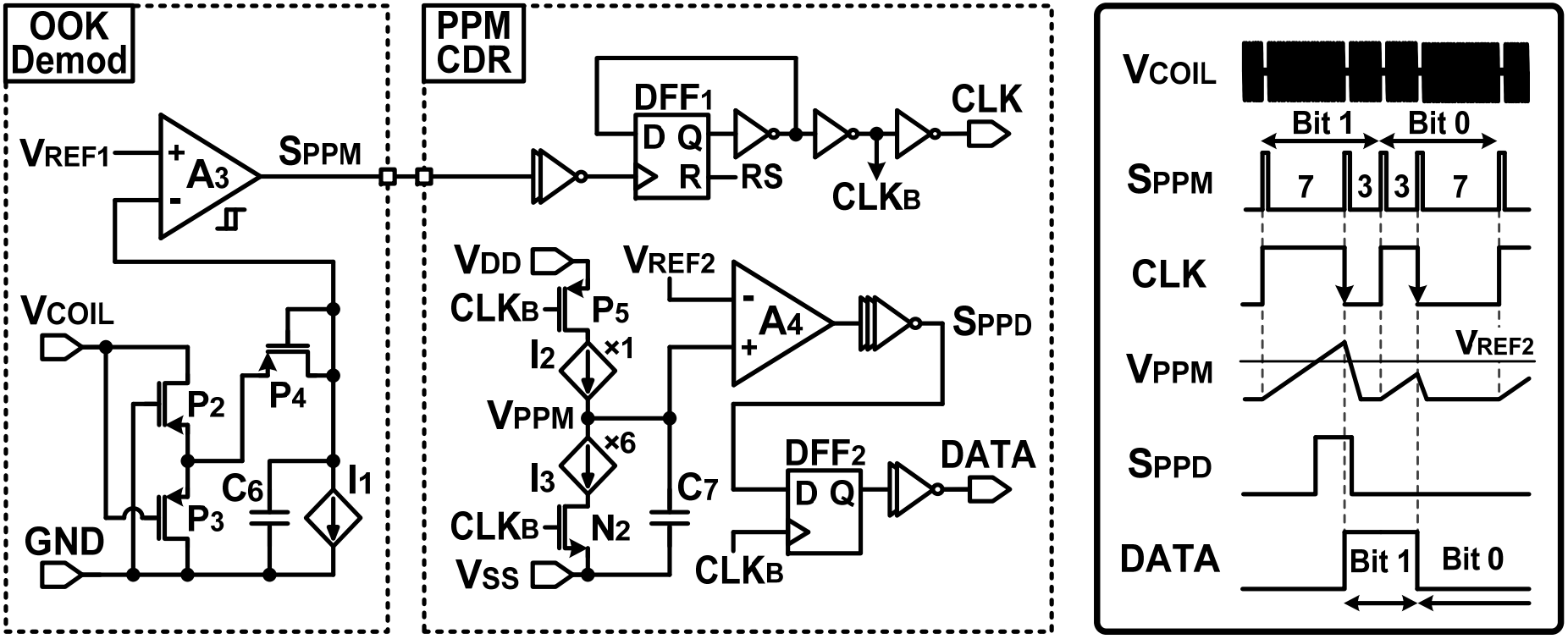




- Injected charge detection → Discharged capacitor voltage
- CM adaptively stops stimulation when charges are balanced.
- Offset cancellation in C_5

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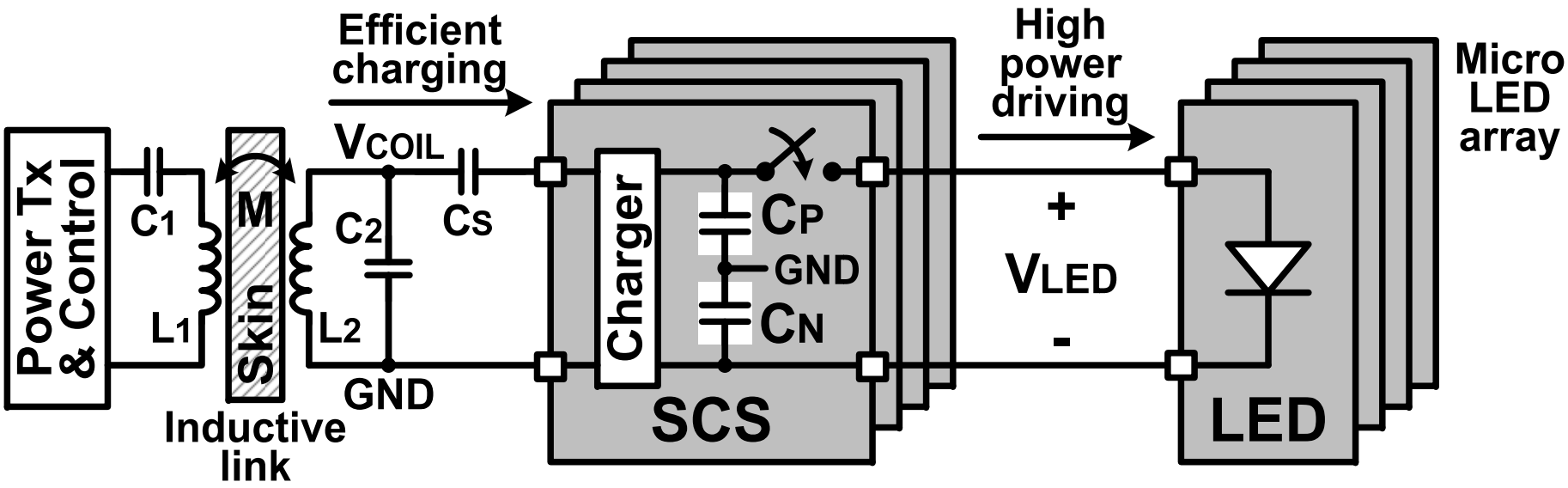
Forward Data Telemetry



- On-off-keying (OOK) demodulator → signal extraction
- Pulse-position-modulated clock/data recovery (PPM-CDR) → synchronized clock and data

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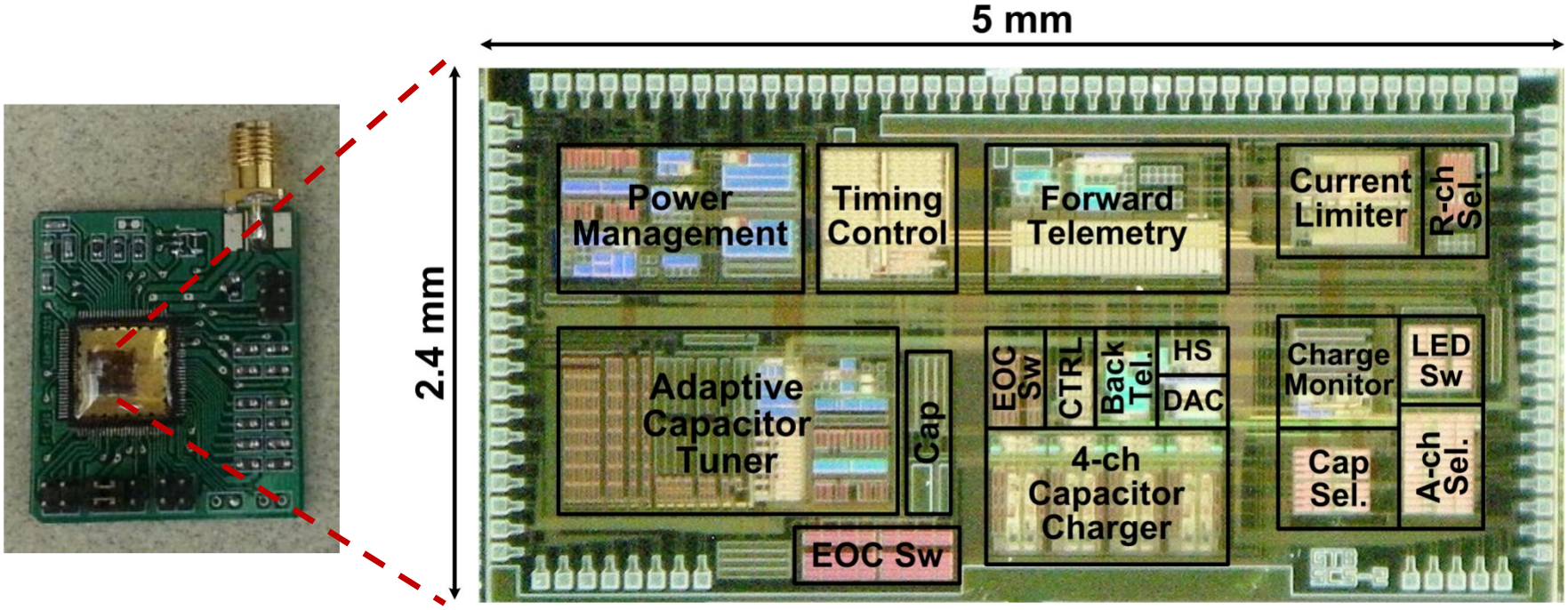
Wireless Optogenetics with SCS



- High instantaneous current without degrading link coupling and system supply
- Discharging storage capacitors into micro-LED arrays periodically to emit sufficient light

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SCS System-on-a-Chip Prototype



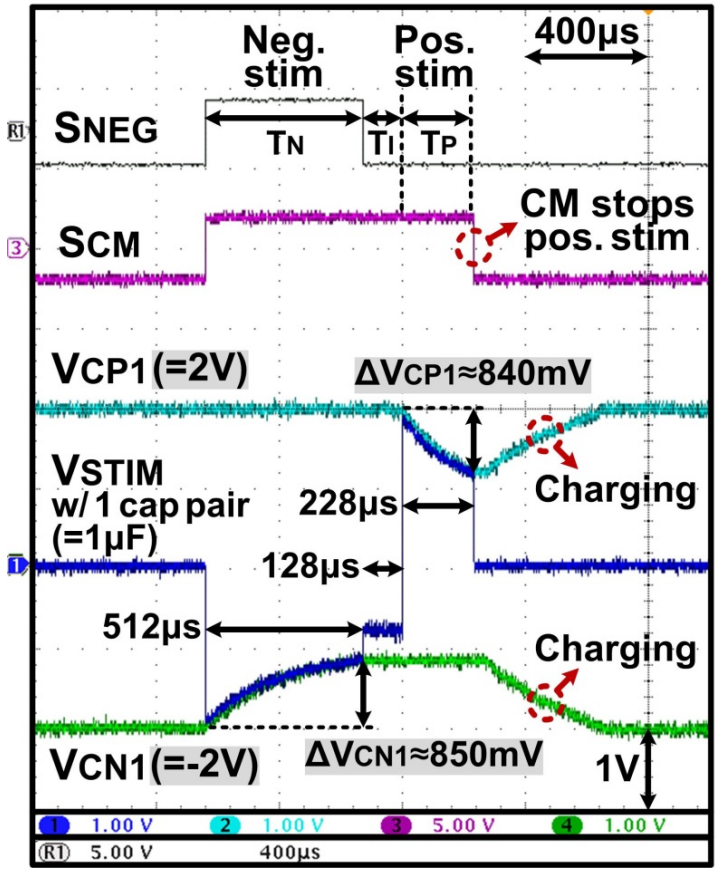
[SCS prototype]

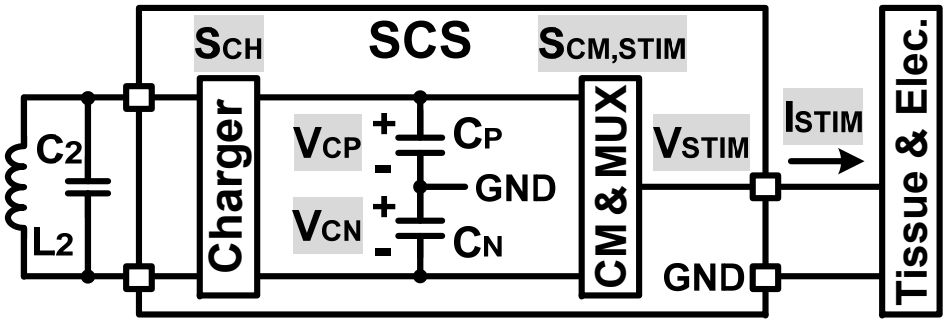
[Chip micrograph and floor plan]

- Process: TSMC 0.35-μm Std. CMOS, *n*-well, 4M2P, 5V
- 4-ch wireless SCS system-on-chip area: 12 mm^2 w/ pads
- 4 pairs off-chip storage caps (1μF), $1 \times 0.5 \times 0.5$ mm^3 each

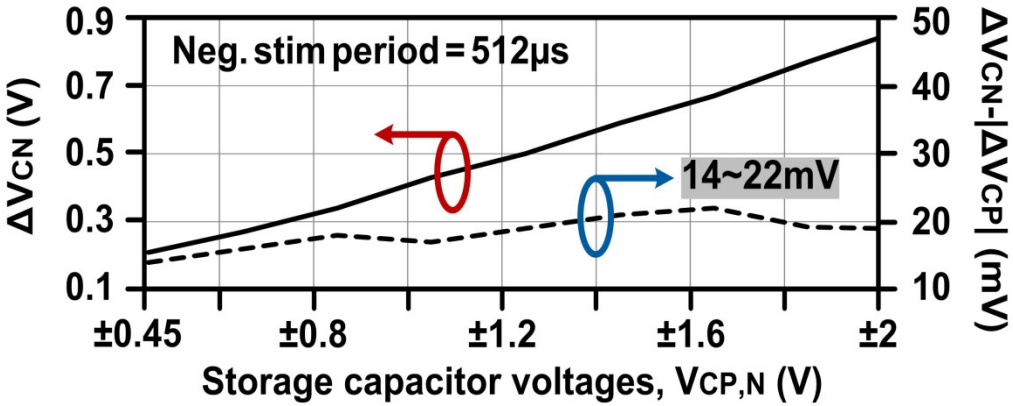
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Charge Monitoring Measurements





[Simplified SCS system]



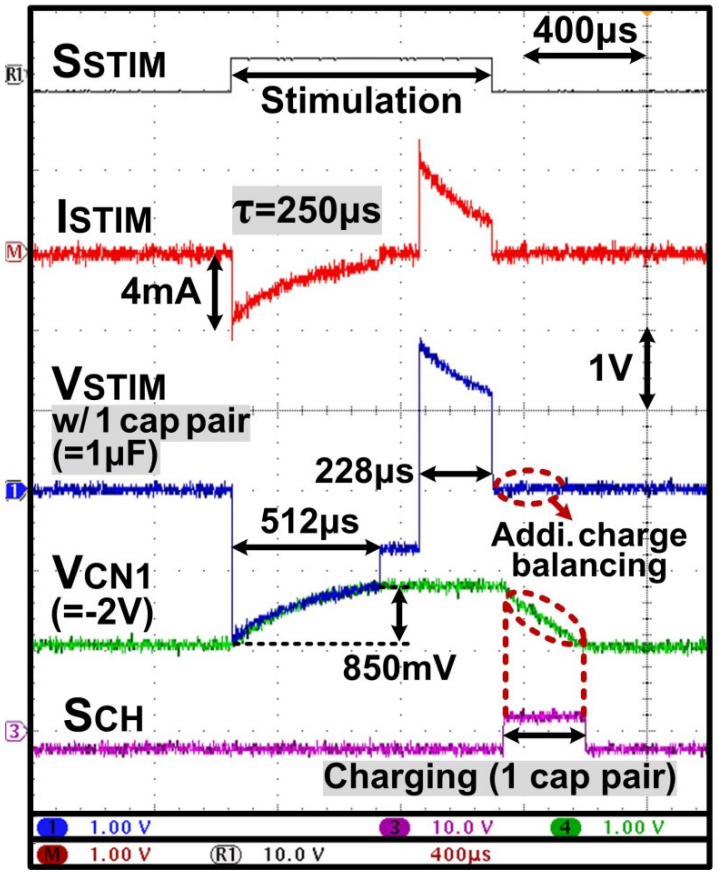
[Discharged voltage mismatch]

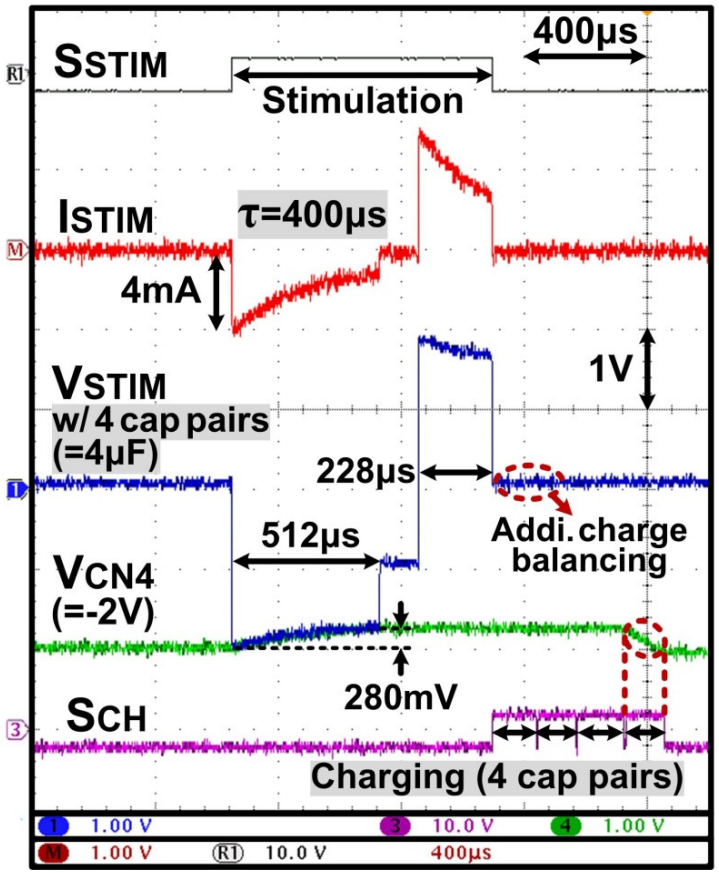
- After 512µs cathodic phase, anodic period is dynamically adjusted to 228µs for charge balancing.
- Discharged voltage mismatch = 2.2% with ±2V capacitors.

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Overall SCS System Measurements

1μF



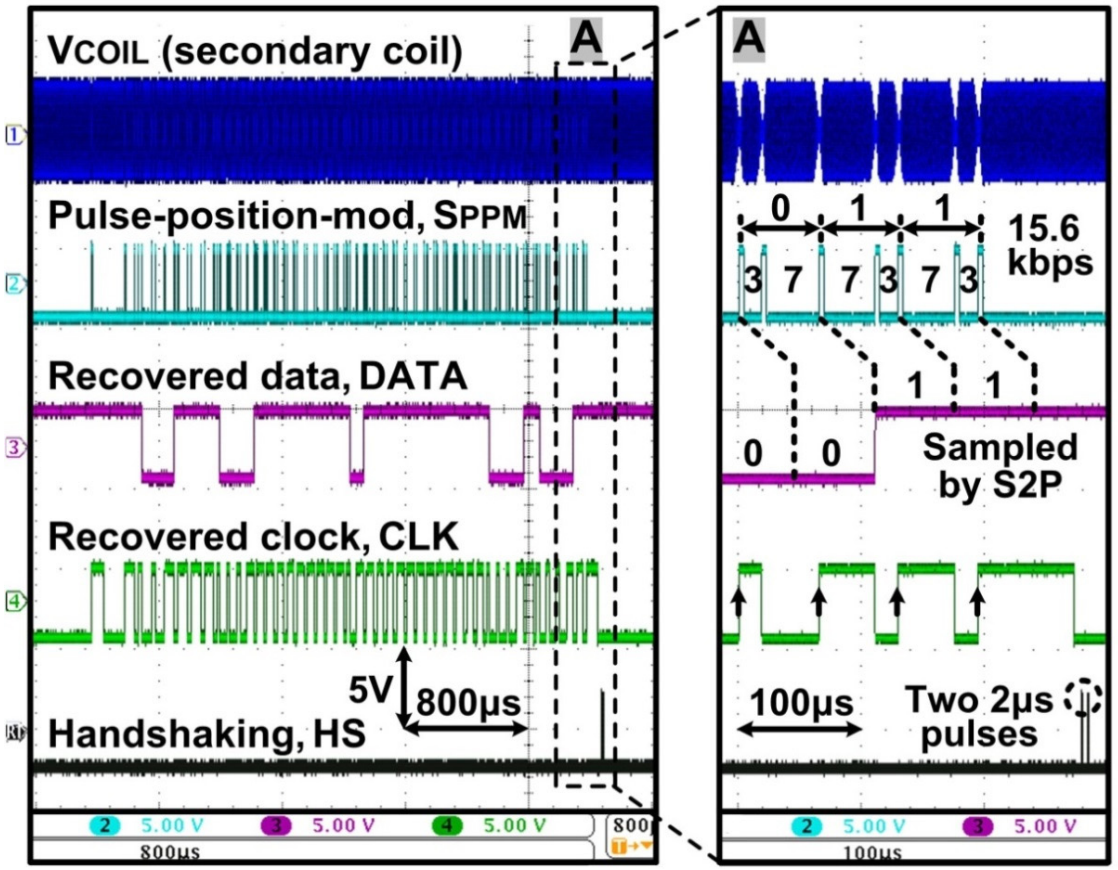


4μF

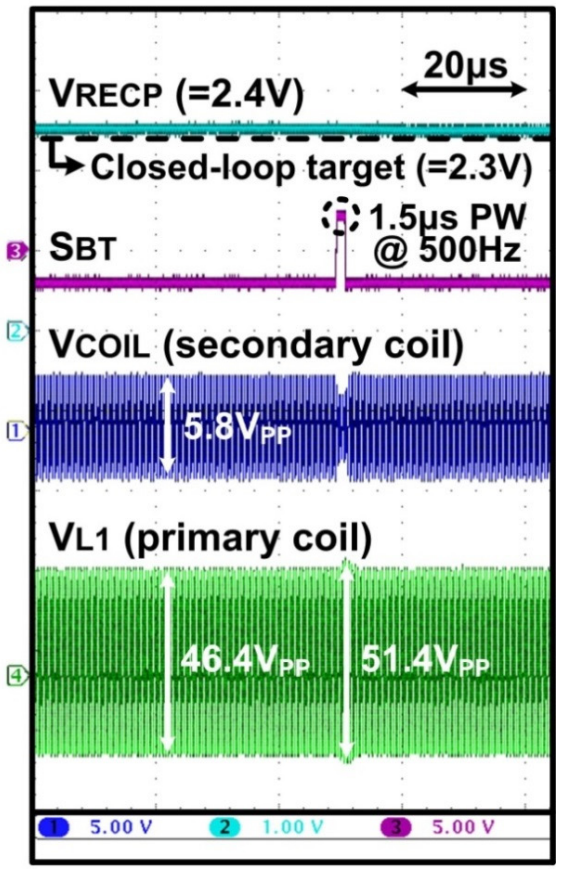
- The decaying-exponential stimulus shape is adjustable.
- Sequential charging & additional passive charge balancing

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Forward/Back Telemetry Measurements



[Forward telemetry]



[Back telemetry]

- OOK-PPM forward telemetry → Stimulation parameters
- LSK back telemetry → Closed-loop inductive power control

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Performance Comparison/Summary

Publication		Chen, JSSC'10	Arfin, TBCAS'12	Kelly, TBCAS'11	This work
Technology		0.18µm HV	0.35µm	1.5µm	0.35µm
Stim. structure		CCS	VCS + CCS	SCS	SCS
Supply volt. (V)		±12	3.3	±1.75 (cap)	±2 (cap)
Stimu-lator power eff. (%)	Rec / Reg	85.6	80*	-	-
	DC-DC	-	55 ~ 94	-	-
	I-driver	41.6	-	-	-
	Charger+Sw	-	-	40**	80.4
	Total	35.6	44 ~ 75.2	40	80.4
Stimulus shape		Rectangular	Rectangular	Decaying expo.	Decaying expo.
Max. *ISTIM* (mA)		0.5	0.45	0.4 (peak)	4 (peak)
Series RC model		10kΩ + 100nF	1kΩ + 0.93µF	1.15kΩ + 0.98µF	0.5kΩ + 1µF

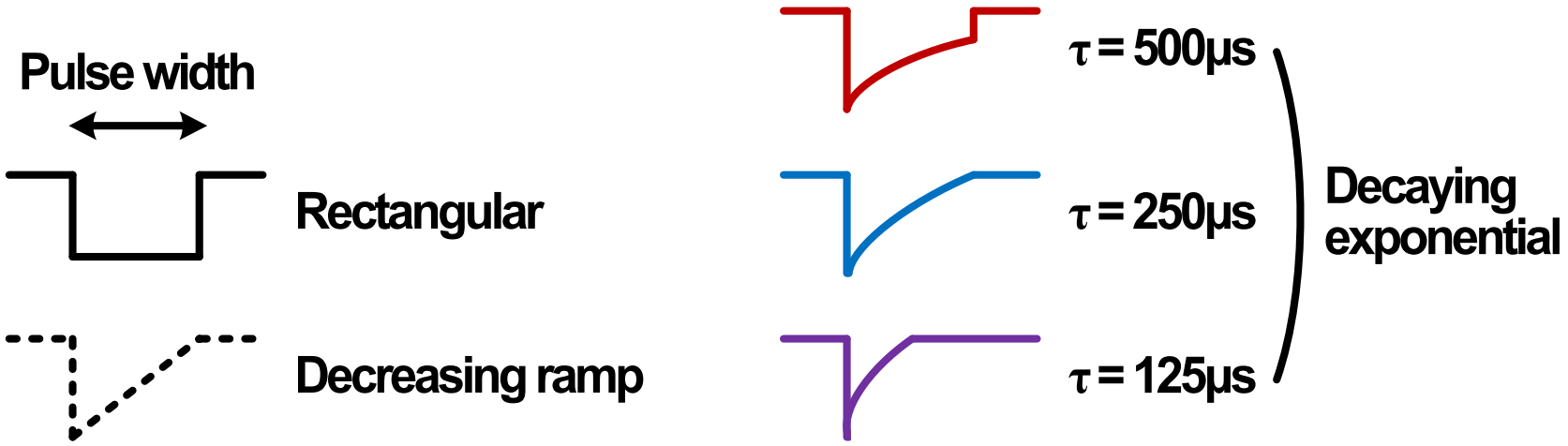
*Considered the rectifier only, **Including power consumption of other blocks.

Overall system		Switched-capacitor stimulation	
L1 / *L2* / *fc*	4µH / 1.2µH / 2MHz	# of channels	4 (active) + 4 (return)
ASIC area	12mm^2	Stimulation freq.	7.6 ~ 244Hz (5b)
System supply	2.1V / -2.1V	Pulse width	16 ~ 512µs (5b)
Inductive capacitor charger		Charge balancing	C-monitor + passive
Target voltages	±0.45 ~ ±2V (5b)	\|*QNEG*\| - *QPOS*	< 22nC
INL / DNL	0.44 / 0.24 LSB	Current limiter	0.012 ~ 1.5mA (5b)*
\|*VCN*\| - *VCP*	< ±26mV	Forward data telemetry	
Charging eff. / time	45~82% / 40~420µs	Data/preamb. bits	40b / 8b
CS / *CP* / *CN*	1nF / 1µF / 1µF	PPM data rate	15.6kbps

* No limiting option available.

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Energy-Efficient Stimulus Waveforms

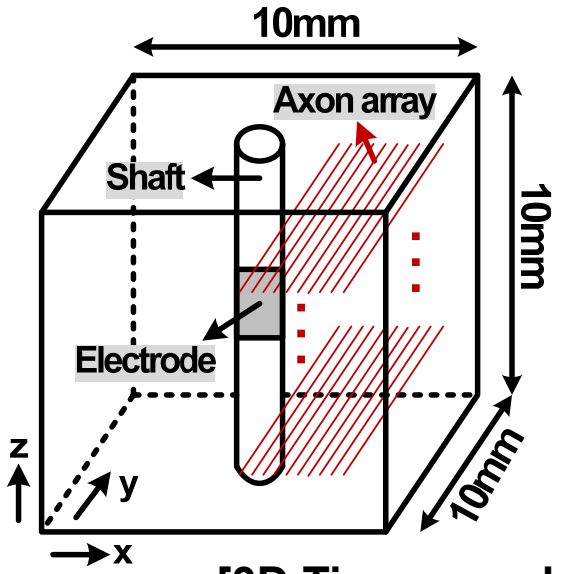


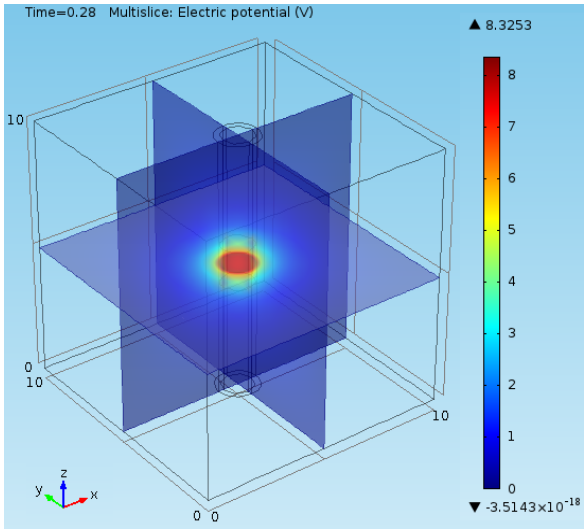
[Various stimulus waveforms]

- Stimulus waveform shapes affect overall stimulation efficacy.
- Target stimulus waveform
 → More effective in activating the neural tissue
 → Less stimulus energy consumption

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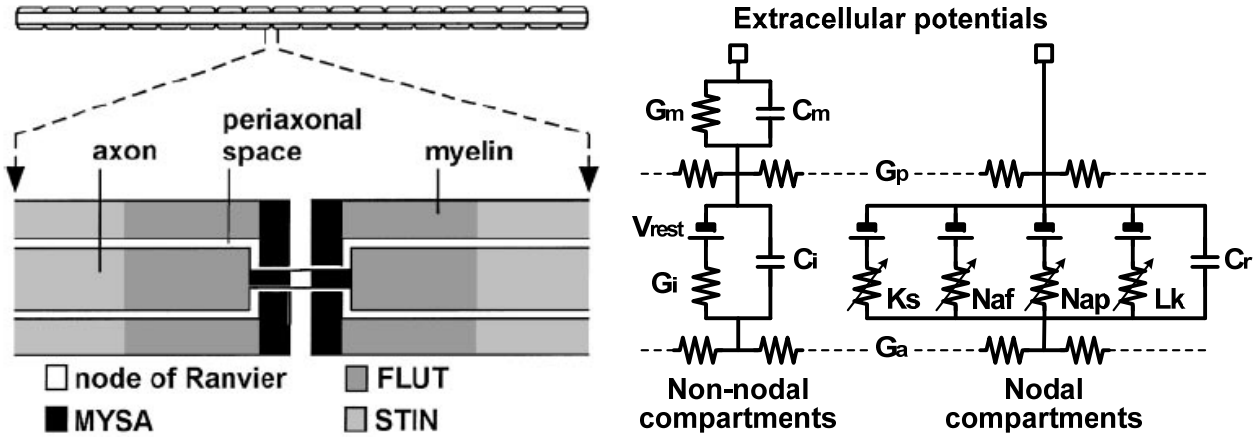
Tissue and Axonal Model





[3D Tissue model with axon arrays]

- Assumption: axons are uniformly distributed in tissue.
- Injected stimuli lead to time-domain field potentials in the tissue.



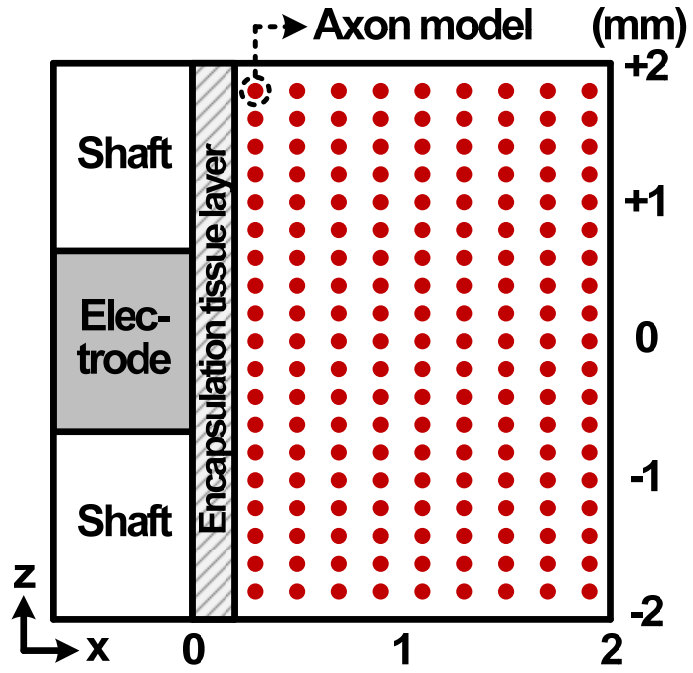
[Multi-compartment double-cable axon model]

McIntyre & Grill, *J. Neurophysiol.*'02

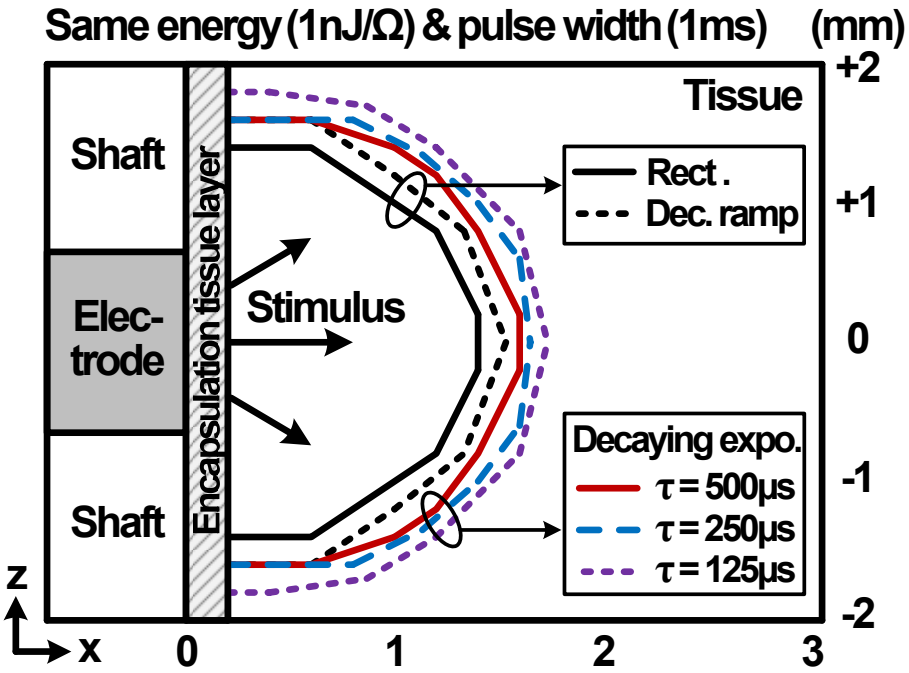
- Extracellular potentials in axon arrays increase transmembrane potential in each axon.

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Area of Tissue Activated



[Cross-section of tissue model with uniform axon array]



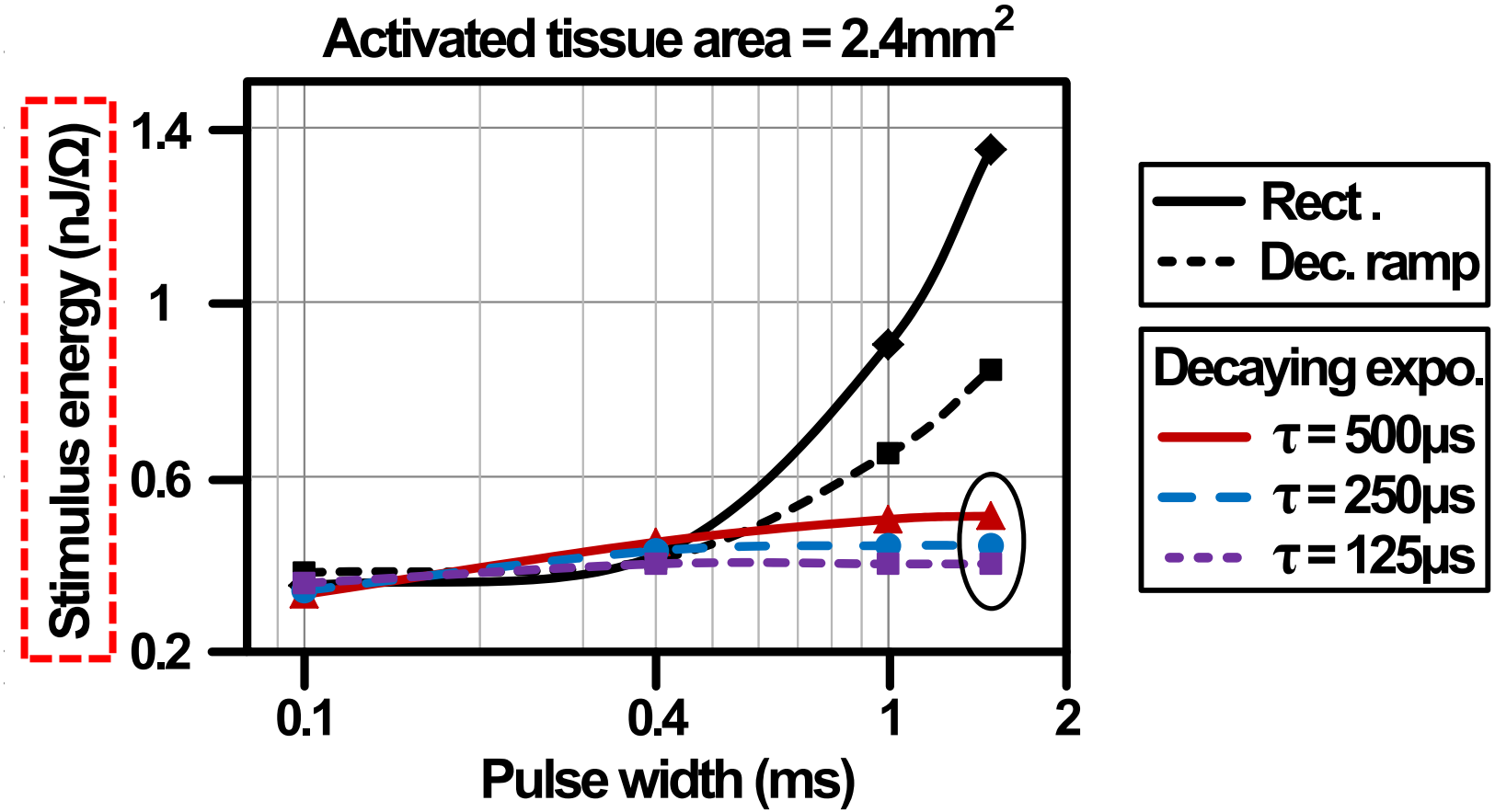
[Area of tissue activated by various stimulus waveforms]

- With same stimulus energy (1nJ/Ω) & pulse width (1ms),

→ the decaying exponential with smaller time constant can activate larger tissue area than other stimulus waveforms.

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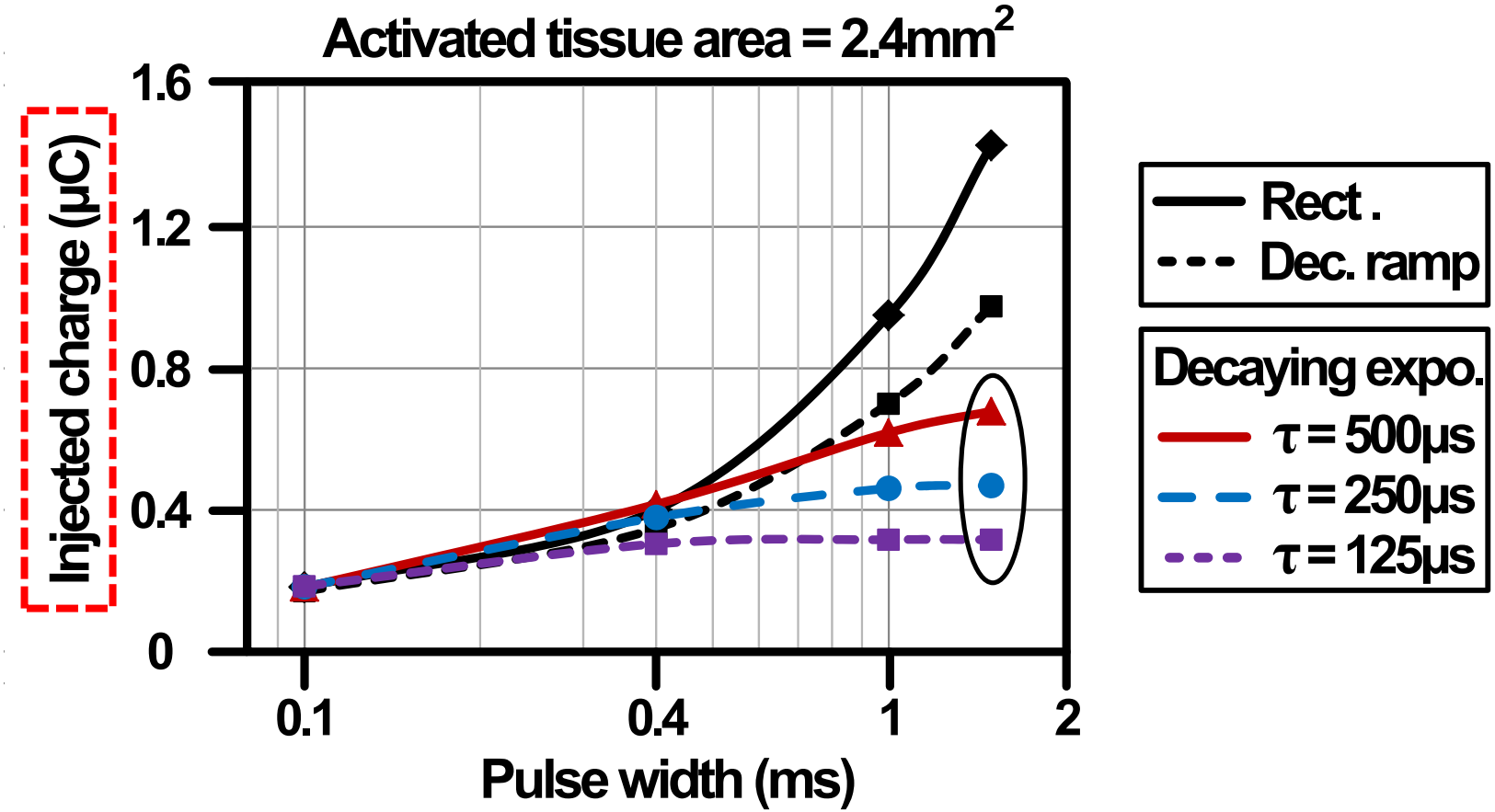
Model Simulation Results (1/3)



- Large PW → Decaying expo. requires smaller stimulus energy.
 → Energy-efficient stimulation
- Small PW → All waveforms show similar stimulus efficacy.

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Model Simulation Results (2/3)

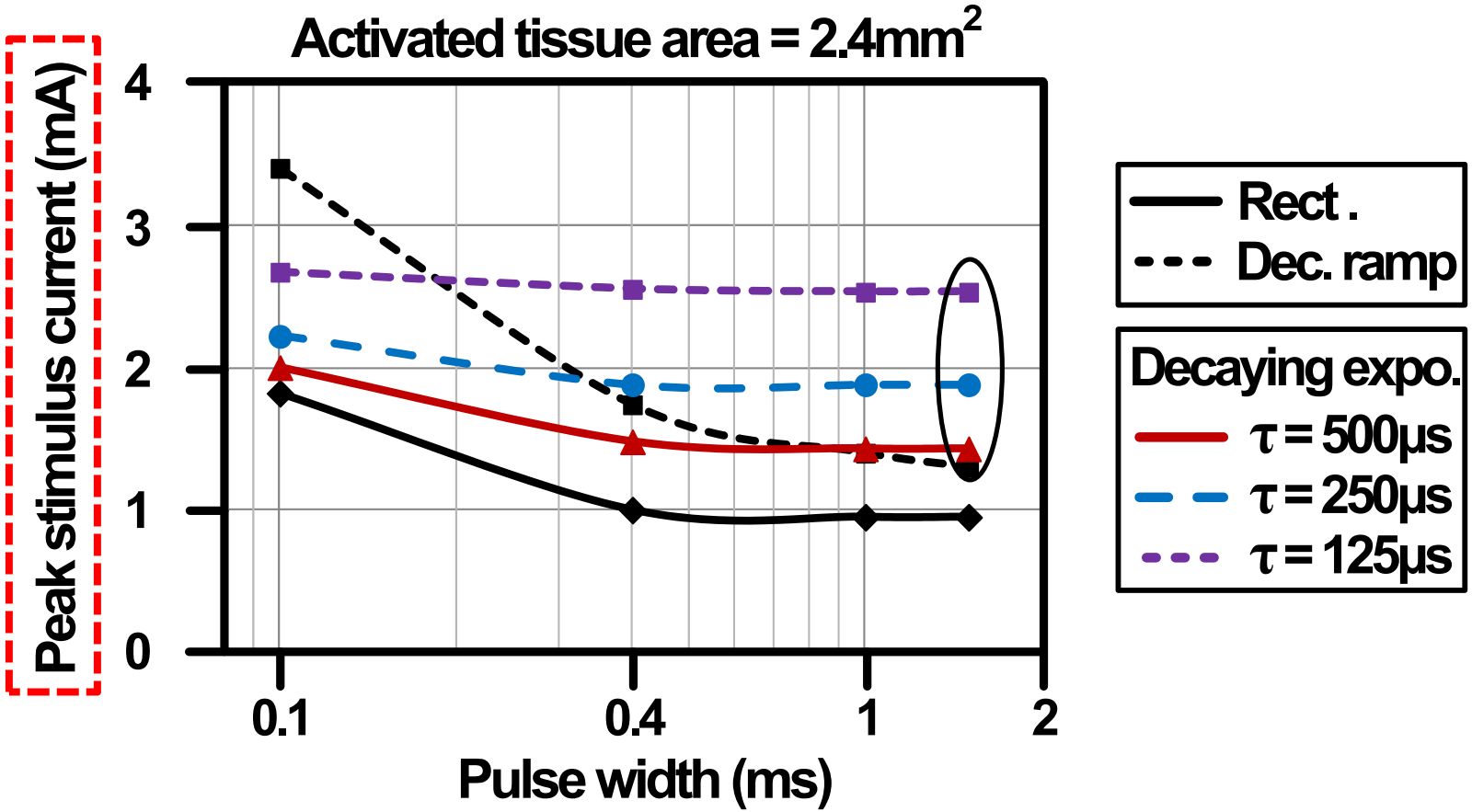


- Decaying expo. requires less injected charge.

→ Safe and effective stimulation

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Model Simulation Results (3/3)

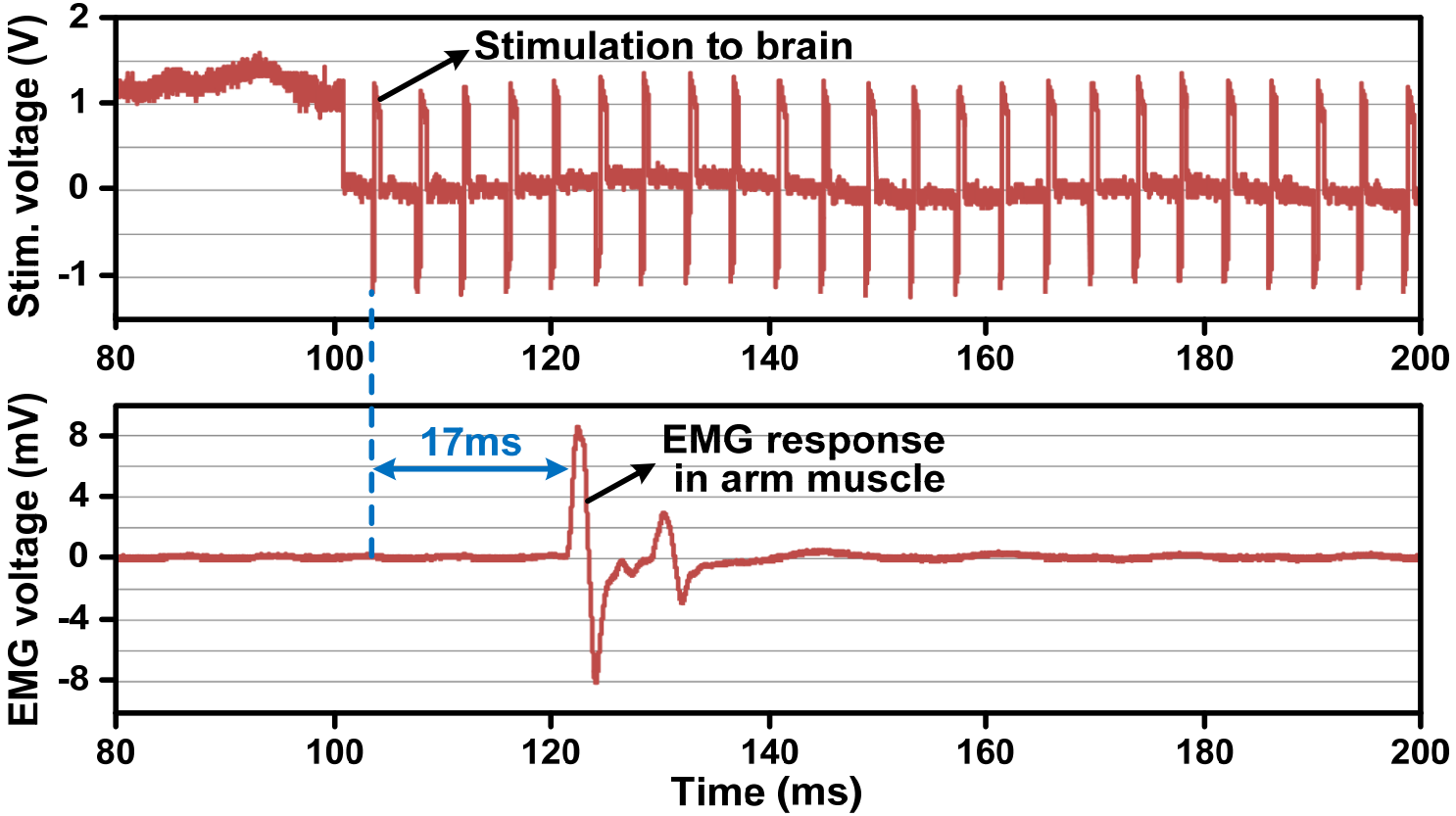


- Decaying expo. requires higher peak stimulus amplitude.

→ Storage capacitors can be charged to higher voltages.

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In Vivo Electrical Stimulation Setup

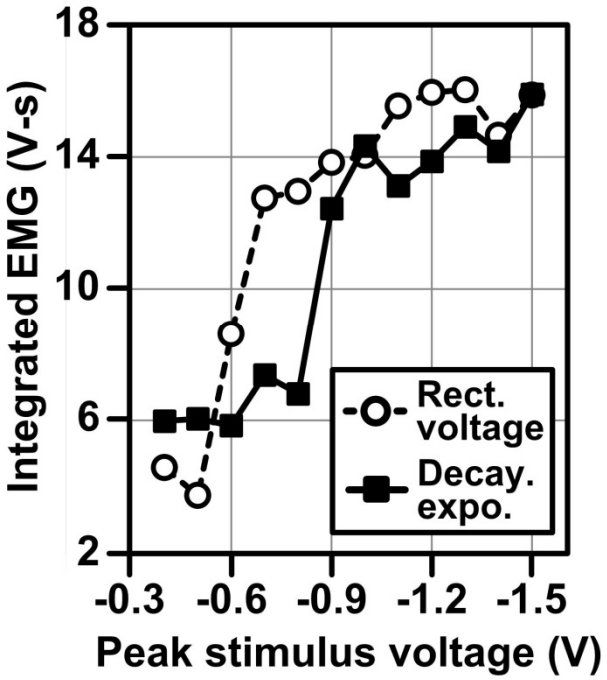


- Stimulation with the SCS system to the posterior limb of internal capsule in the brain of an anesthetized cat
- Electromyography (EMG) recording from upper arm muscle
- 30 biphasic pulses at 244Hz w/ 272μs cathodic & 700μs anodic

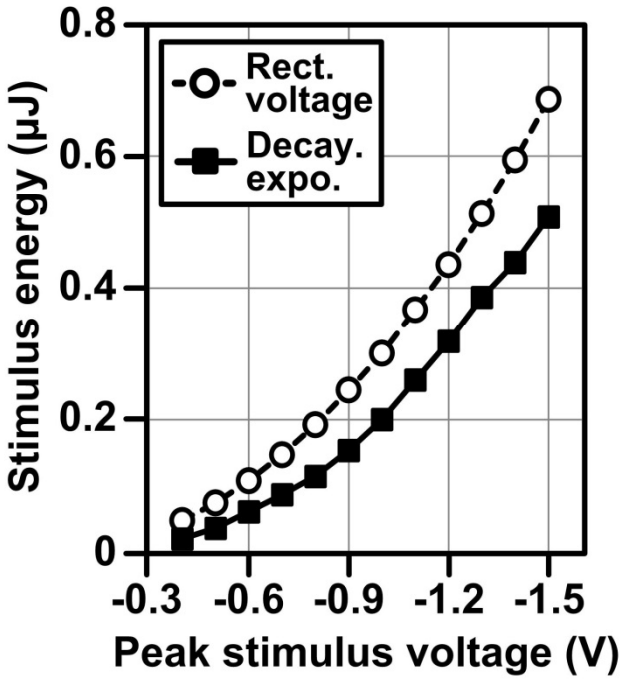
*In collaboration with Prof. W. Grill and B. Howell at Duke University

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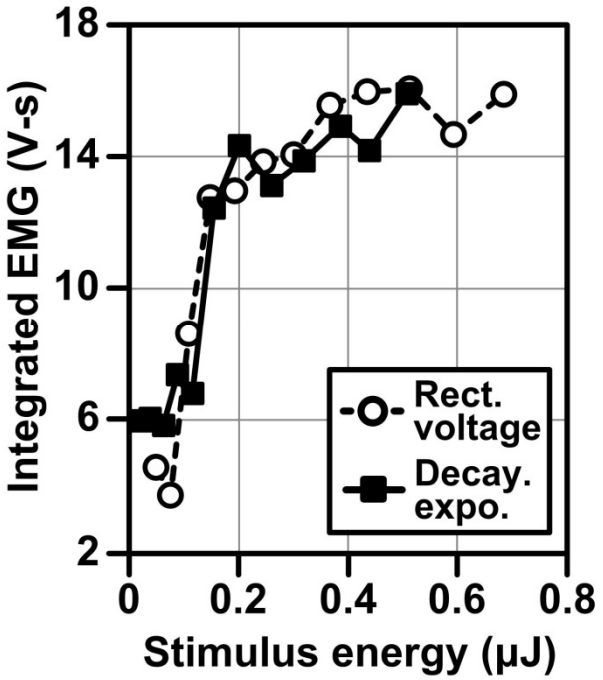
In Vivo Electrical Stimulation Results



[Integrated EMG vs. peak amplitude]



[Stimulus energy vs. peak amplitude]

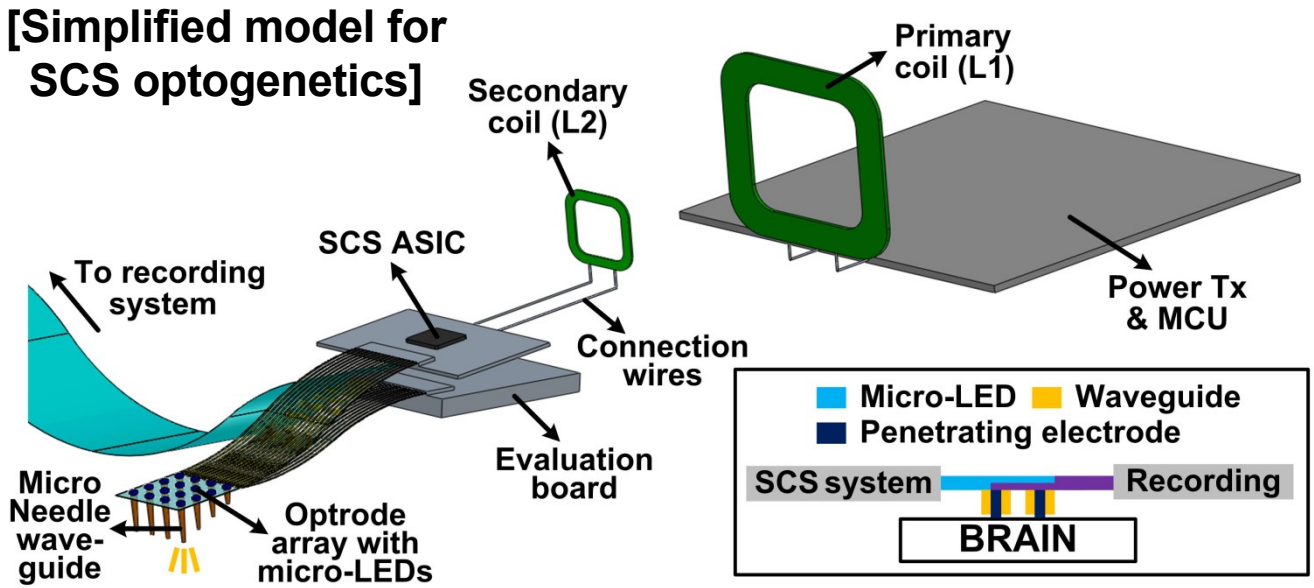


[Integrated EMG vs. Stimulus energy]

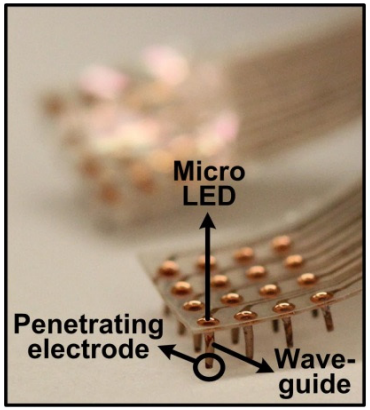
- Decaying exponential vs. rectangular voltage stimulus
- When providing same stimulus energy at 272us pulse width, both shapes have similar EMG response & stimulus efficacy.

*In collaboration with Prof. W. Grill and B. Howell at Duke University

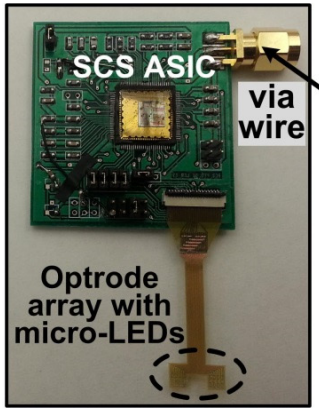
In Vivo Wireless Optogenetics Evaluation



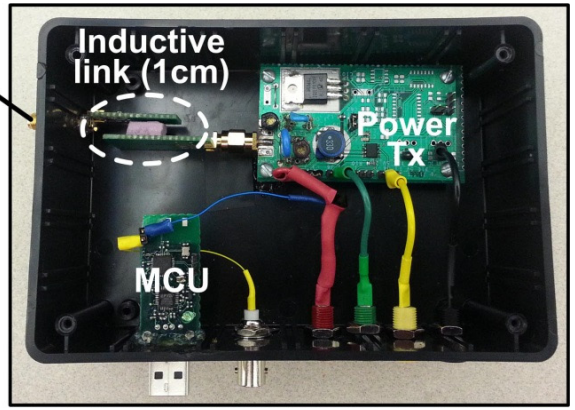
- Wireless power & data via inductive link.
- Optrode array with micro-LEDs (optical stim.) & transparent elect. (neural recording)
- Micro-needle waveguides for light delivery to the tissue.



[Optrode array w/ waveguides]



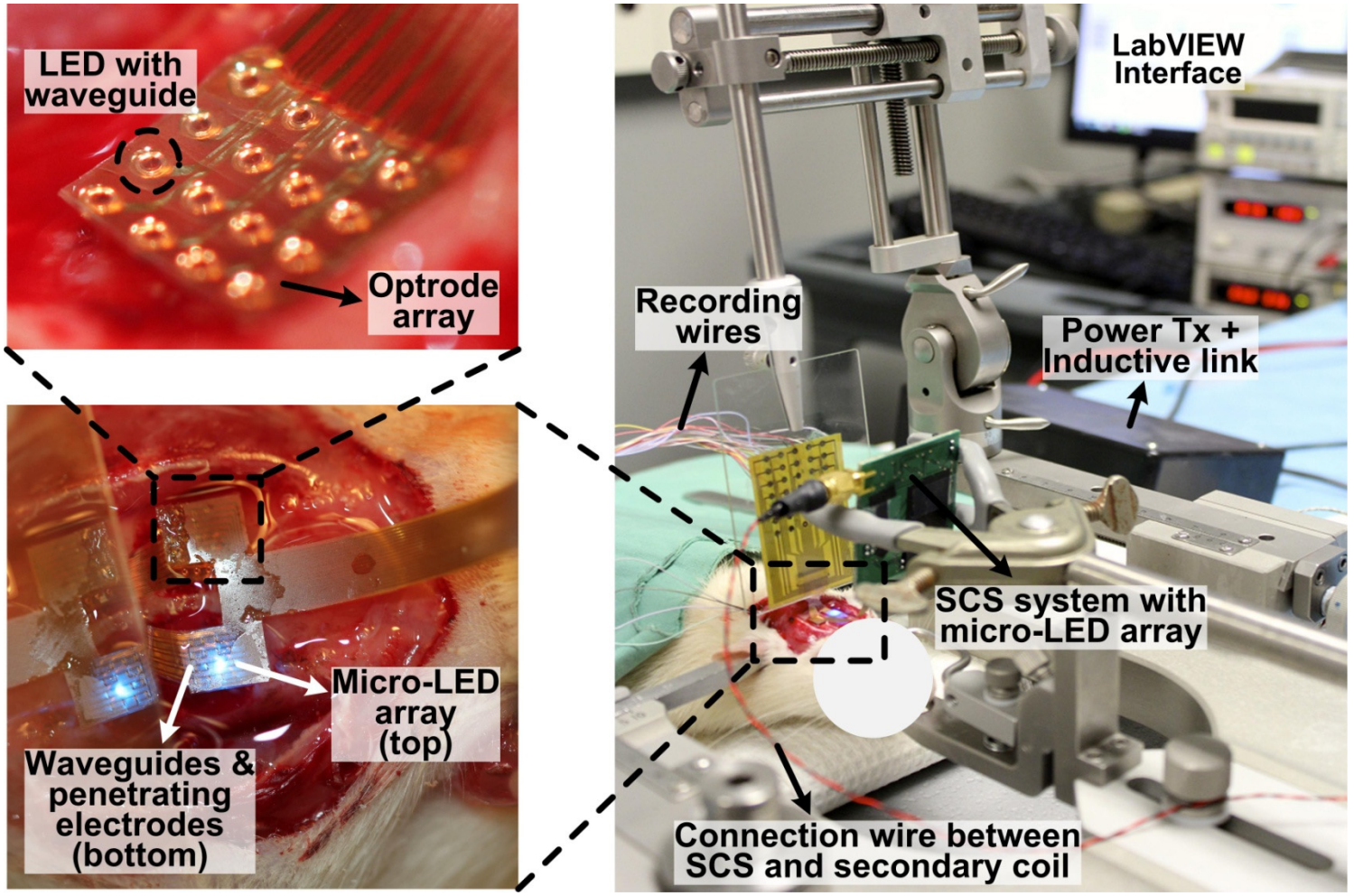
[SCS system w/ optrodes]



[External power Tx w/ inductive link]

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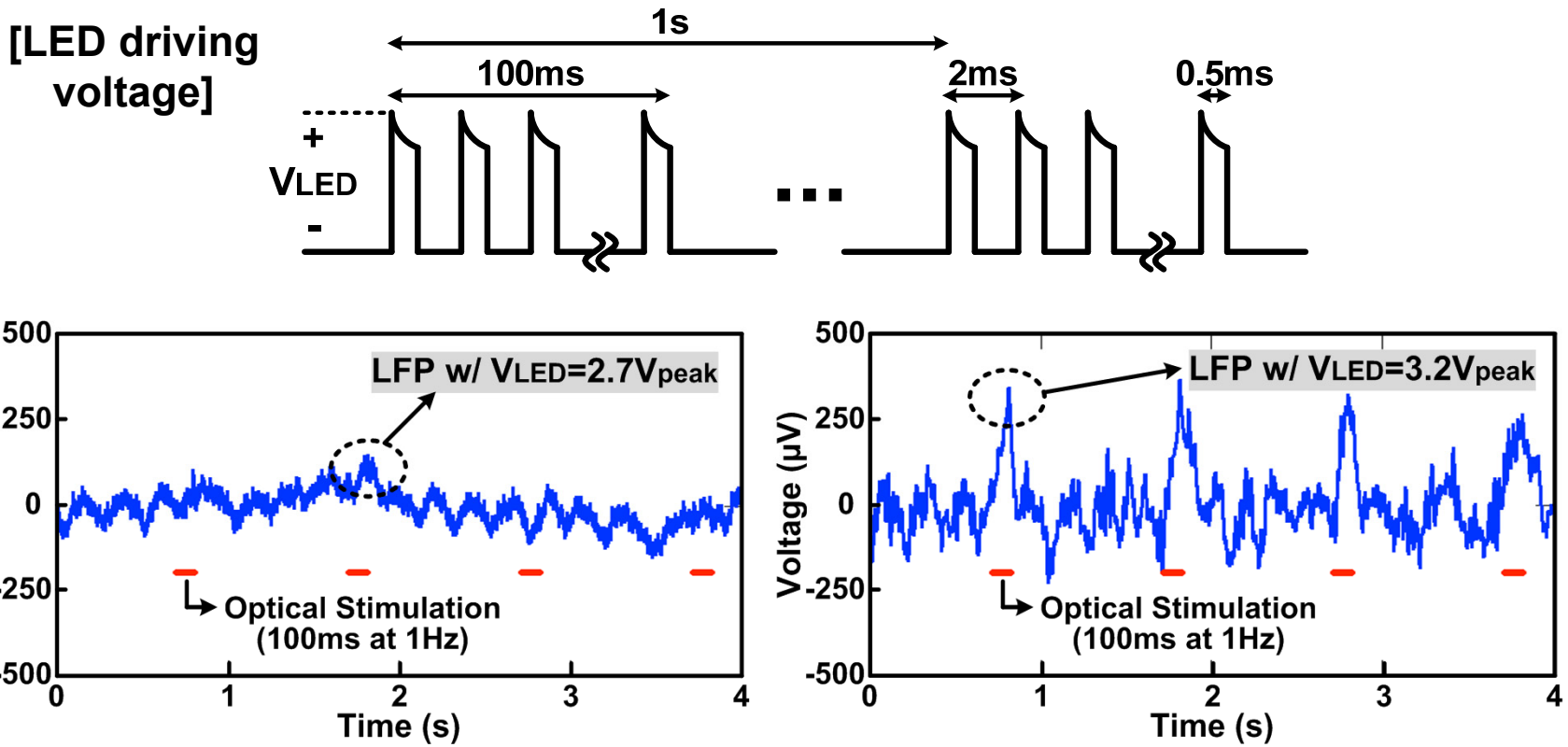
In Vivo Wireless Optogenetics Setup



- Optical stimulation to visual cortex in the brain of anesthetized viral-transfected rats + local field potential (LFP) recording.

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Light-Induced LFP with SCS

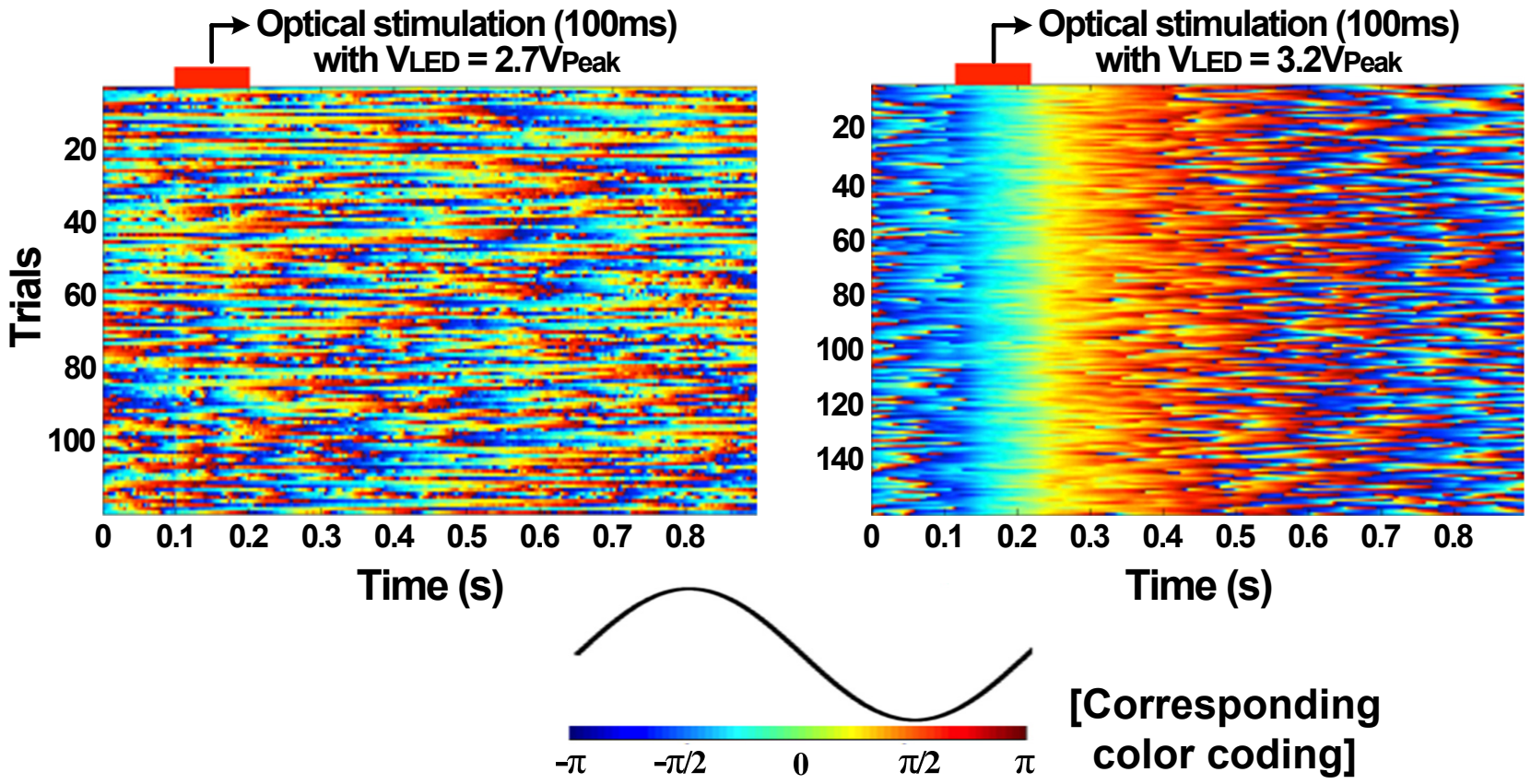


[Light-induced LFP w/ peak V_{LED} = 2.7V and 3.2V]

- Peak LED voltages → 2.7V and 3.2V
- Higher LED voltage delivers sufficient irradiance (>1mW/mm^2) to target tissue, leading to larger light-evoked LFP variation.

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Instantaneous LFP Phase



- Instantaneous phase of light-induced LFP at 1~25Hz
- No phase consistency w/ V_{LED} = 2.7V_{Peak}, while clear phase synchronization during optical stimulation w/ V_{LED} = 3.2V_{Peak}.

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Conclusions

- Wireless switched-capacitor stimulating (SCS) system
 → High efficiency, high driving capability, and safety
 → Electrical and optical stimulation

- Capacitor charging → High simulator efficiency (before elec.)
 Charge monitoring → Safe charge-based stimulation
 Decaying-exponential → High stimulus efficacy (after elec.)

- SCS wireless optogenetics
 → Optrode arrays and micro-needle waveguides
 → Precise and efficient light delivery

- *In vivo* animal experiments with SCS

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 - National Science Foundation ECCS-0824199

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 - Mehdi Kiani
 - Byunghun Lee
 - Jaemyung Lim
- Michigan State University:
 - Prof. Wen Li
 - Ki-Yong Kwon
- Duke University:
 - Prof. Warren Grill
 - Bryan Howell



www.gtbionics.org

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An Implantable 64nW ECG-Monitoring Mixed-Signal SoC for Arrhythmia Diagnosis

D. Jeon, Y.-P. Chen, Y. Lee, Y. Kim, Z. Foo,
G. Kruger, H. Oral, O. Berenfeld, Z. Zhang,
D. Blaauw, D. Sylvester

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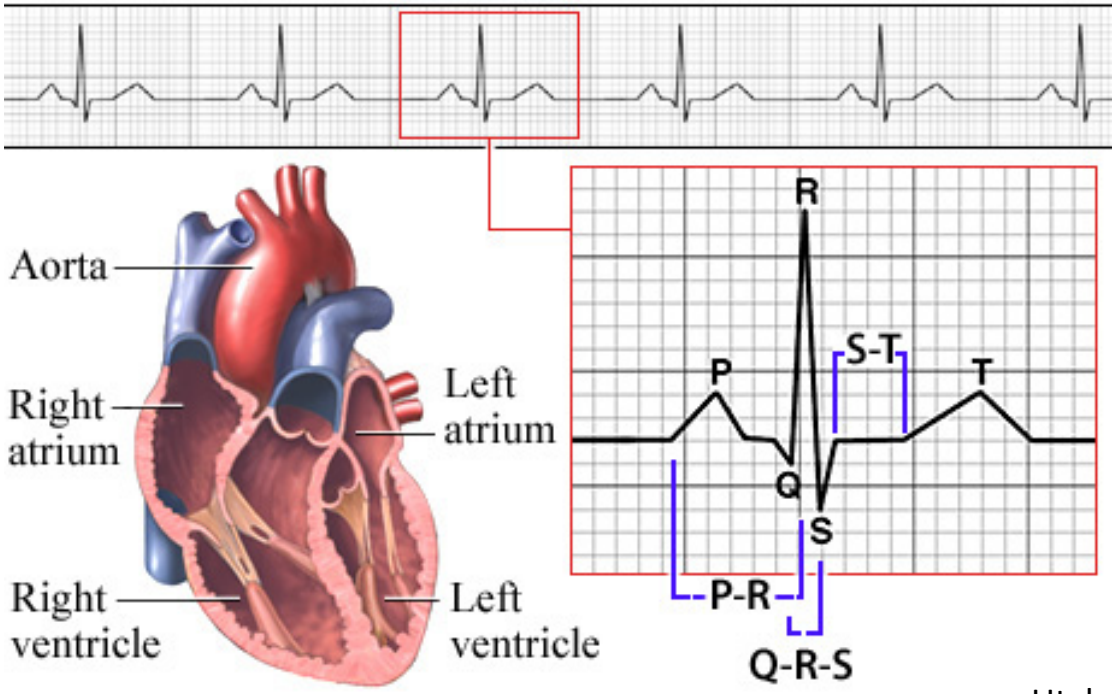
University of Michigan, Ann Arbor



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Electrocardiography (ECG/EKG)

- Electrical activity of heart



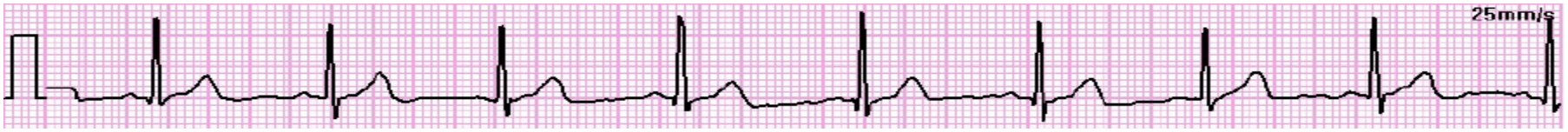
Utah EKG training

- Critical source of information for heart disorders

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Arrhythmia

- Normal Sinus Rhythm



- Arrhythmia
 - Sinus Tachycardia



 - Sinus Arrhythmia



FavoritePlus

- Need to detect peaks and monitor their regularity

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Arrhythmia Monitoring

- Happen infrequently (few times a day)
- Only last seconds to minutes

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Arrhythmia Monitoring

- Happen infrequently (few times a day)
- Only last seconds to minutes

⟹ Long-term observation required!

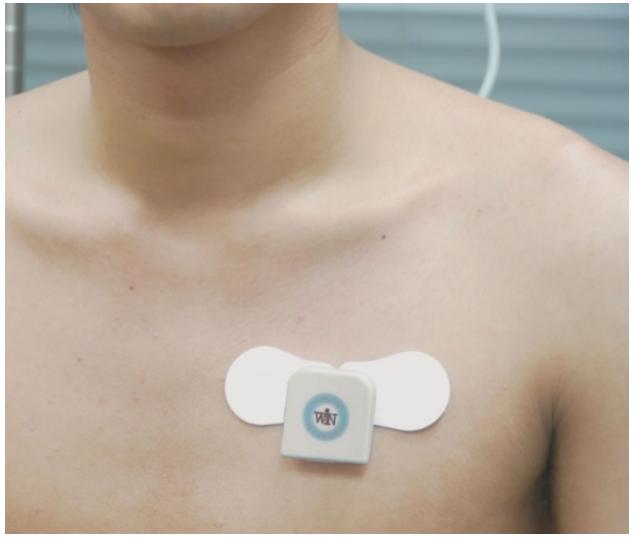
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Arrhythmia Monitoring

- Happen infrequently (few times a day)
- Only last seconds to minutes

 ⟹ Long-term observation required!

- Body-wearable systems
 - Easy to implement
 - Large device size
 - Impact on patient's life
 - Physical contact impedance affected by body movement



WIN Human Recorder Co Ltd

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Arrhythmia Monitoring

- Happen infrequently (few times a day)
- Only last seconds to minutes

 ⇒ Long-term observation required!

- Implanted systems
 - Less impact on patient's life
 - Stable physical contact
 - Less external noise





Medtronic

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Conventional Approach

- Devices implanted by surgery
- Large battery to achieve long lifetime (> years)

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Conventional Approach

- Devices implanted by surgery
- Large battery to achieve long lifetime (> years)

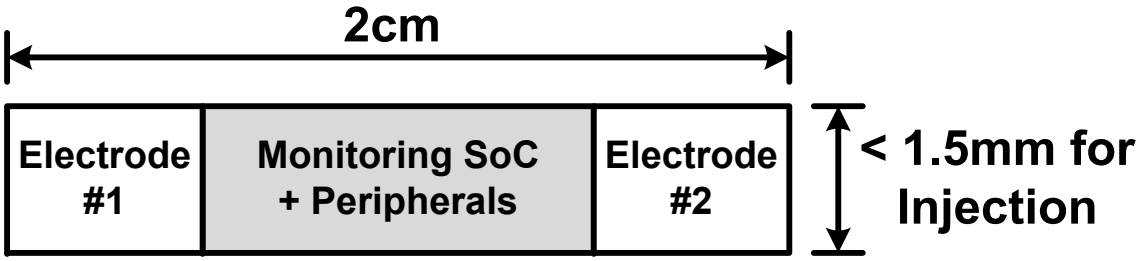
Proposed Approach

- Syringe-implantable small form factor
- Overnight wireless charging and data readout
- <100nW power consumption

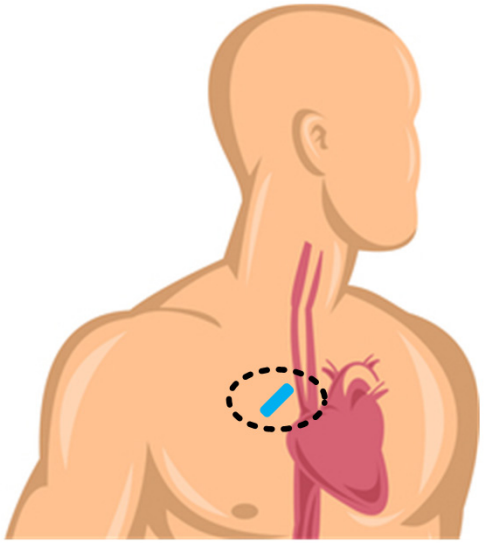
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Syringe-Implantable System

- Small form factor limited by width < 1.5mm
 - Length ∝ signal amplitude



- Injected under skin through syringe needle

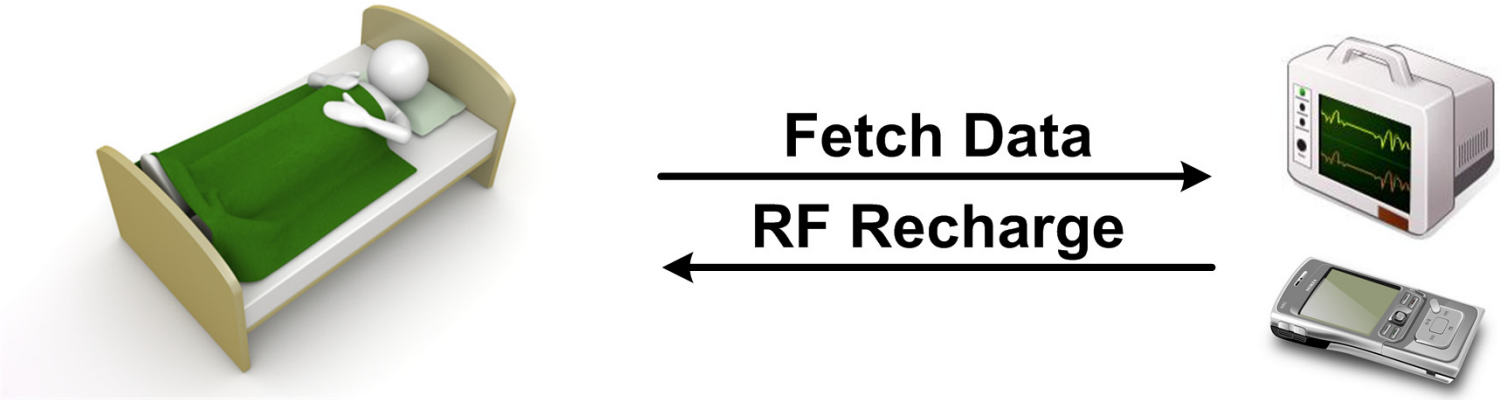


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Use Scenario

- Battery capacity limited by small form factor
- Daily wireless recharging and data readout
 - Lifetime w/o recharge > 5 days (including safe margins)
 - 5μA*hr, 3.7mm^2 Li battery

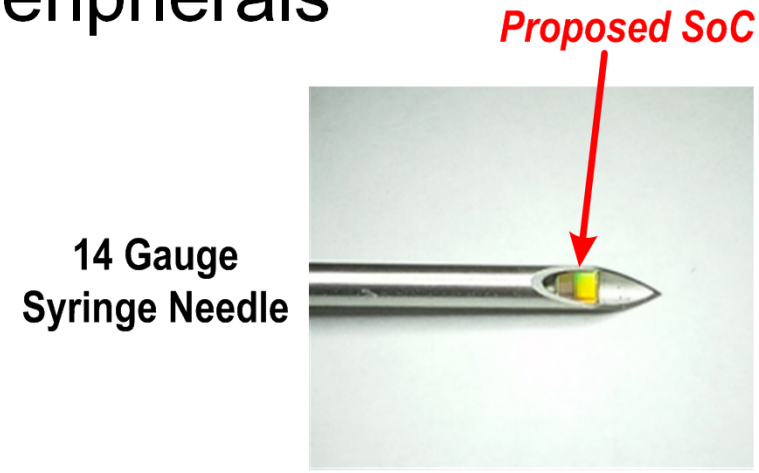
 ⟹ <167nW average power budget

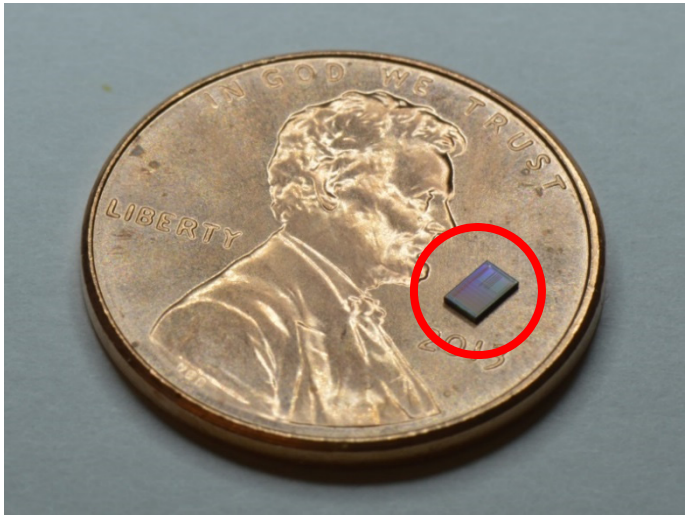


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Proposed System

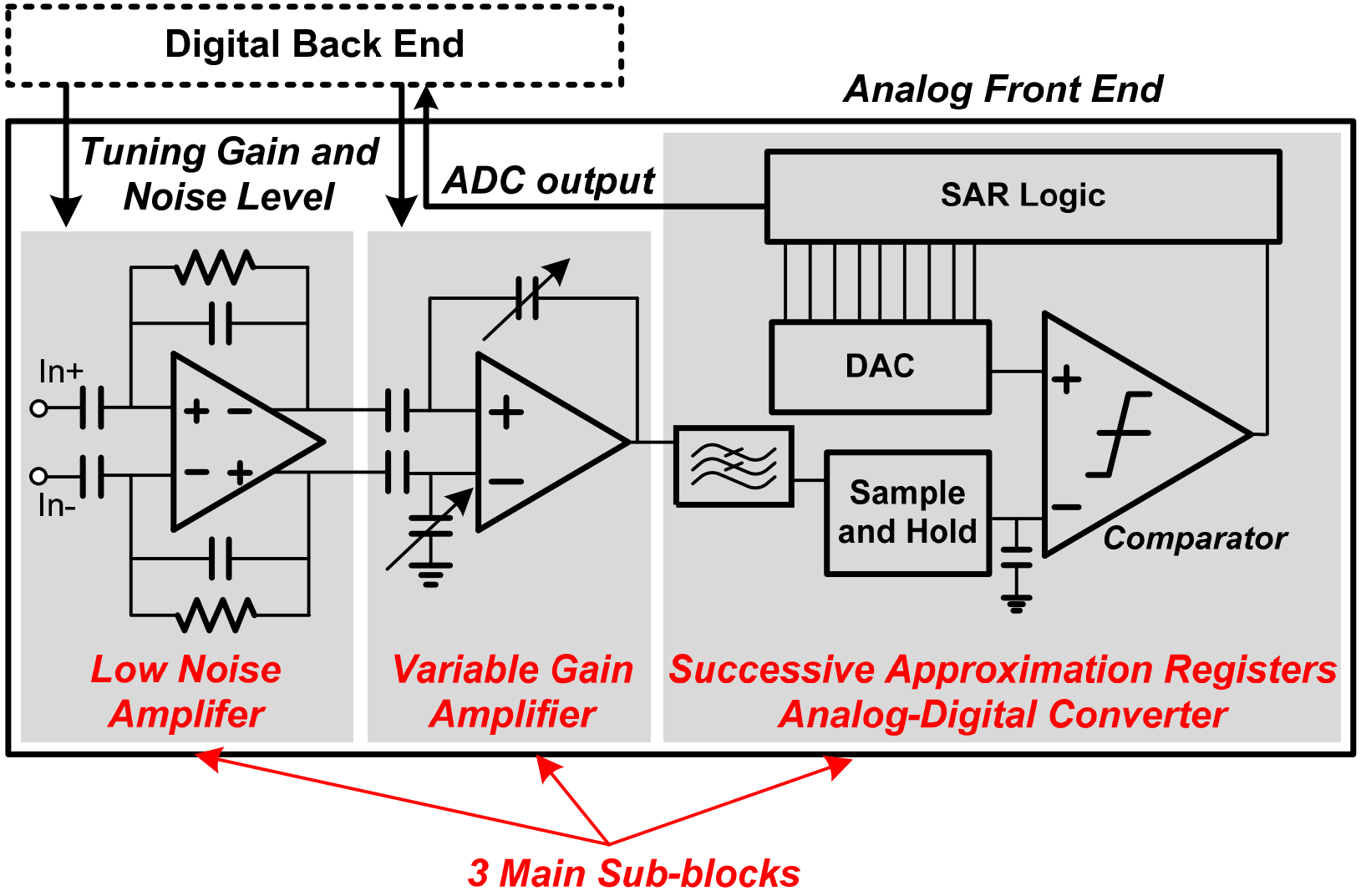
- 1.4mm-wide ECG monitoring SoC
- 64nW total system power
- Analog signal acquisition + DSP
 - Automatic arrhythmia detection
 - Waveform storage
- System demonstration using other ULP sensor node peripherals





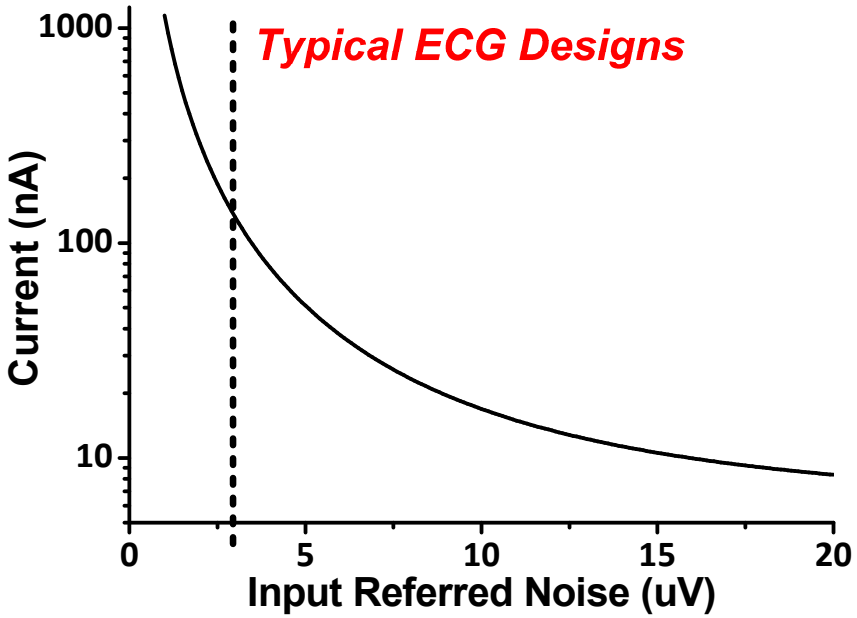
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Analog Front End



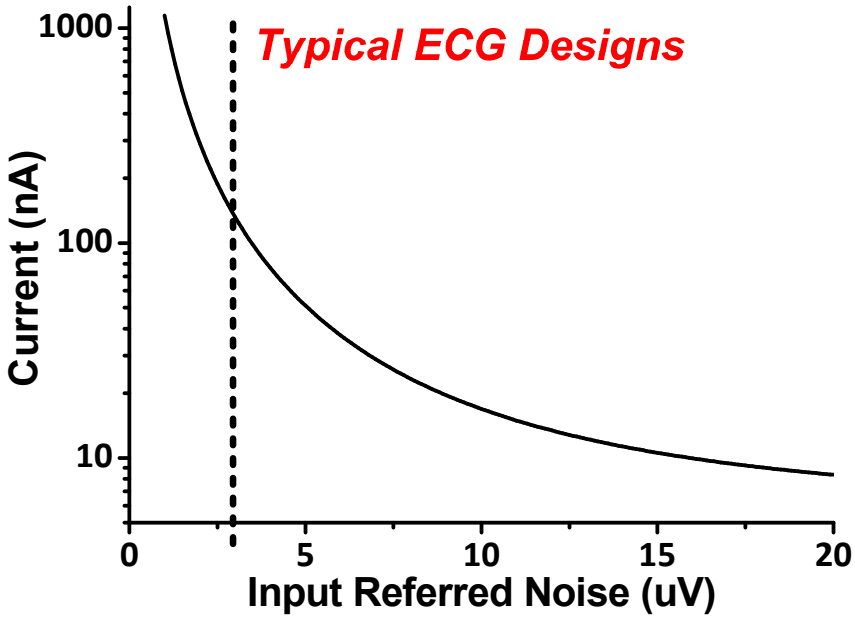
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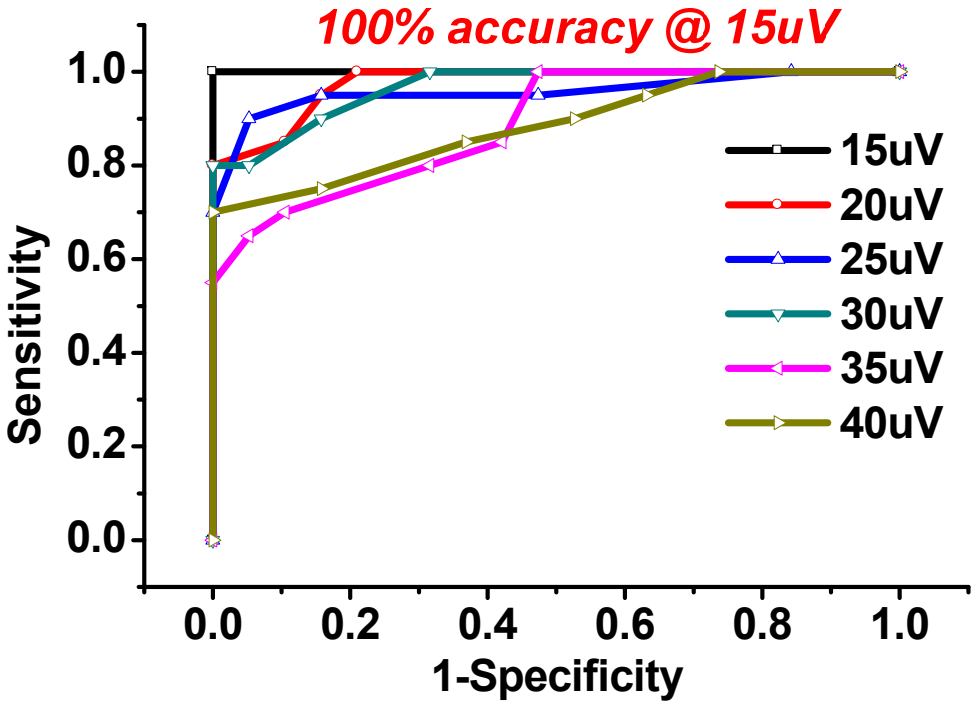
Amplifier Optimization



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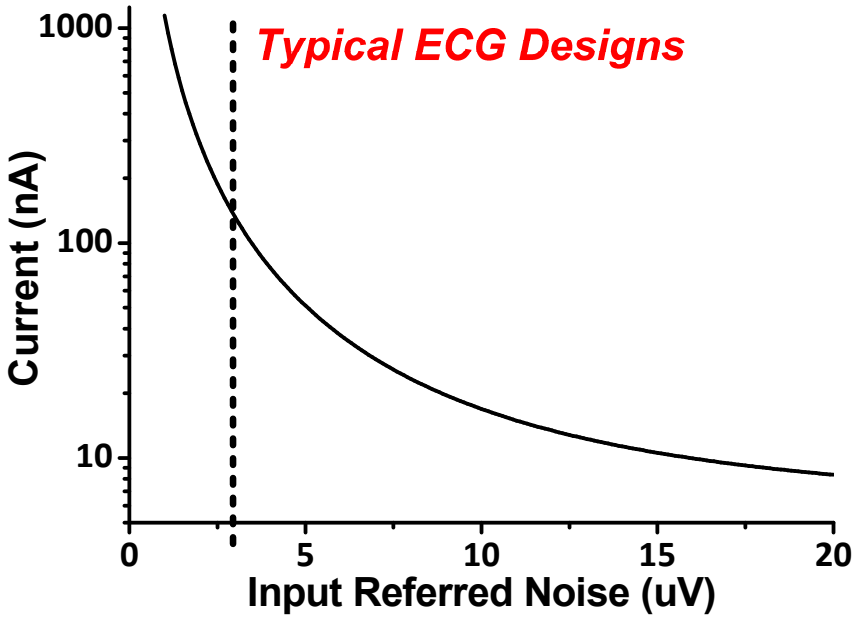
Amplifier Optimization

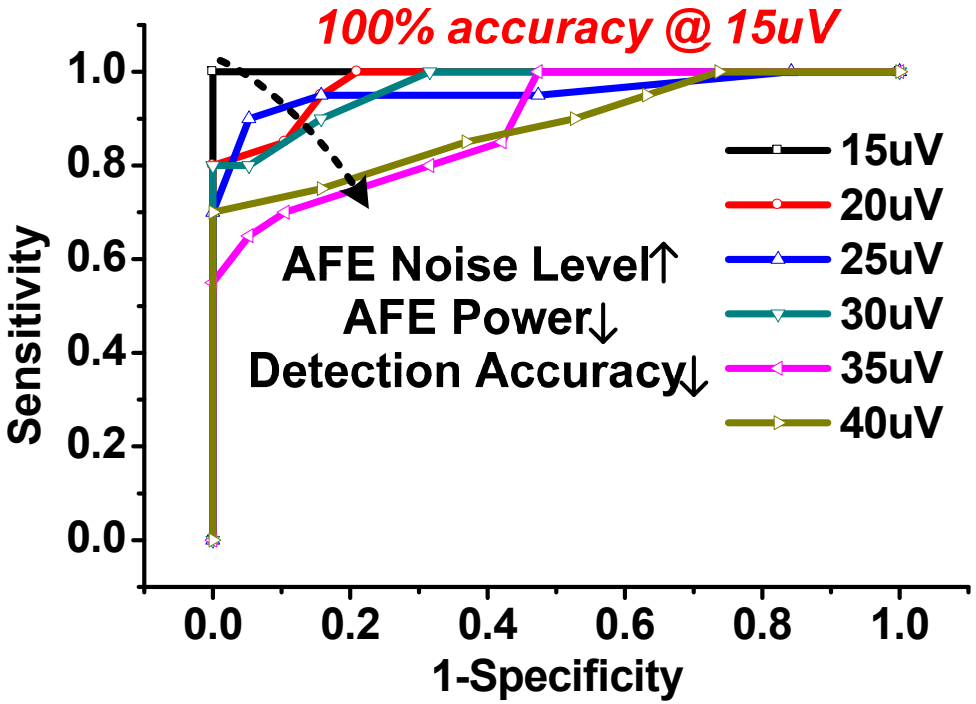




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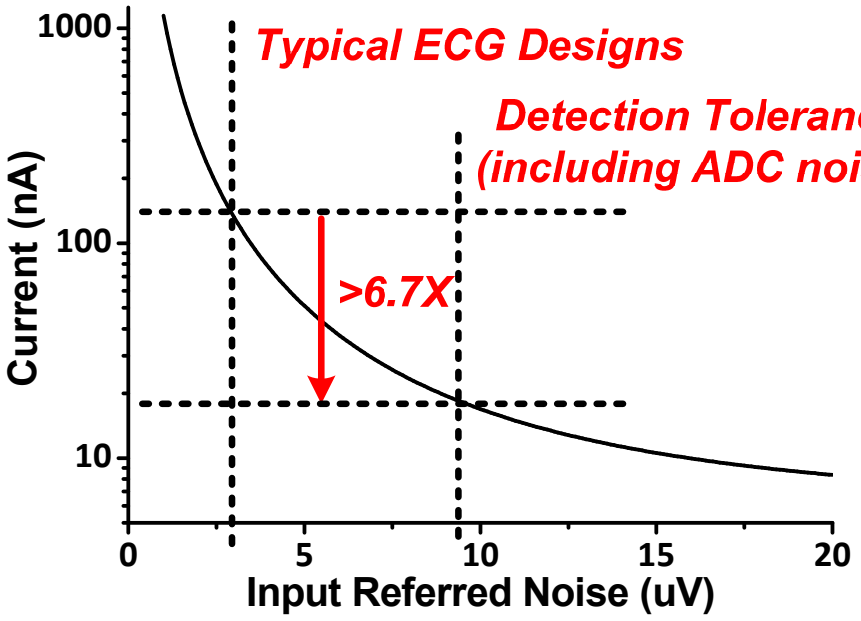
Amplifier Optimization

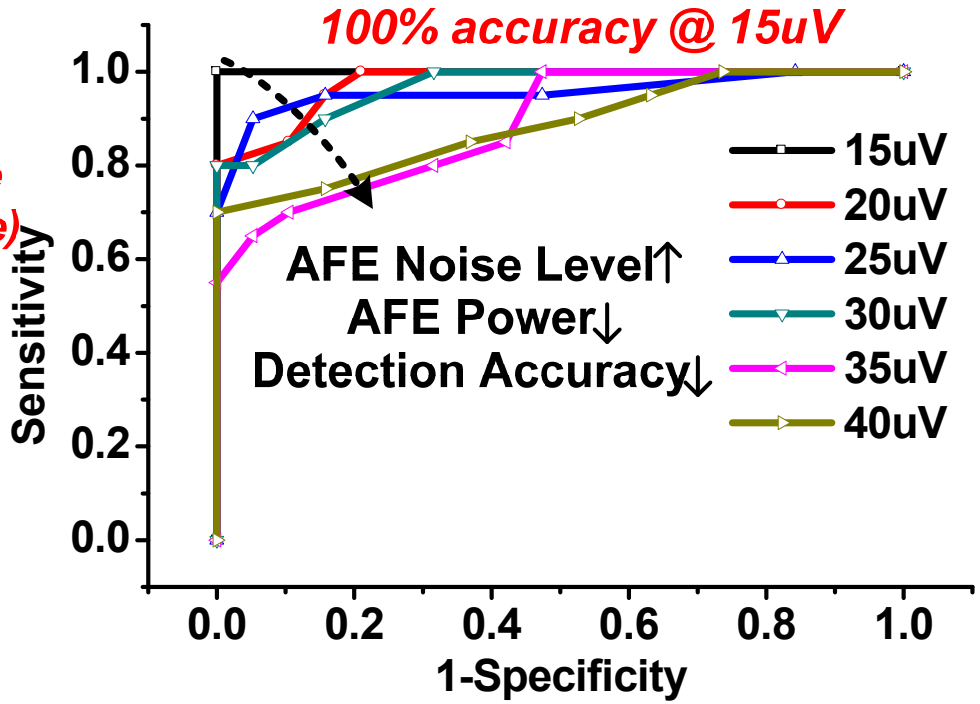




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Amplifier Optimization

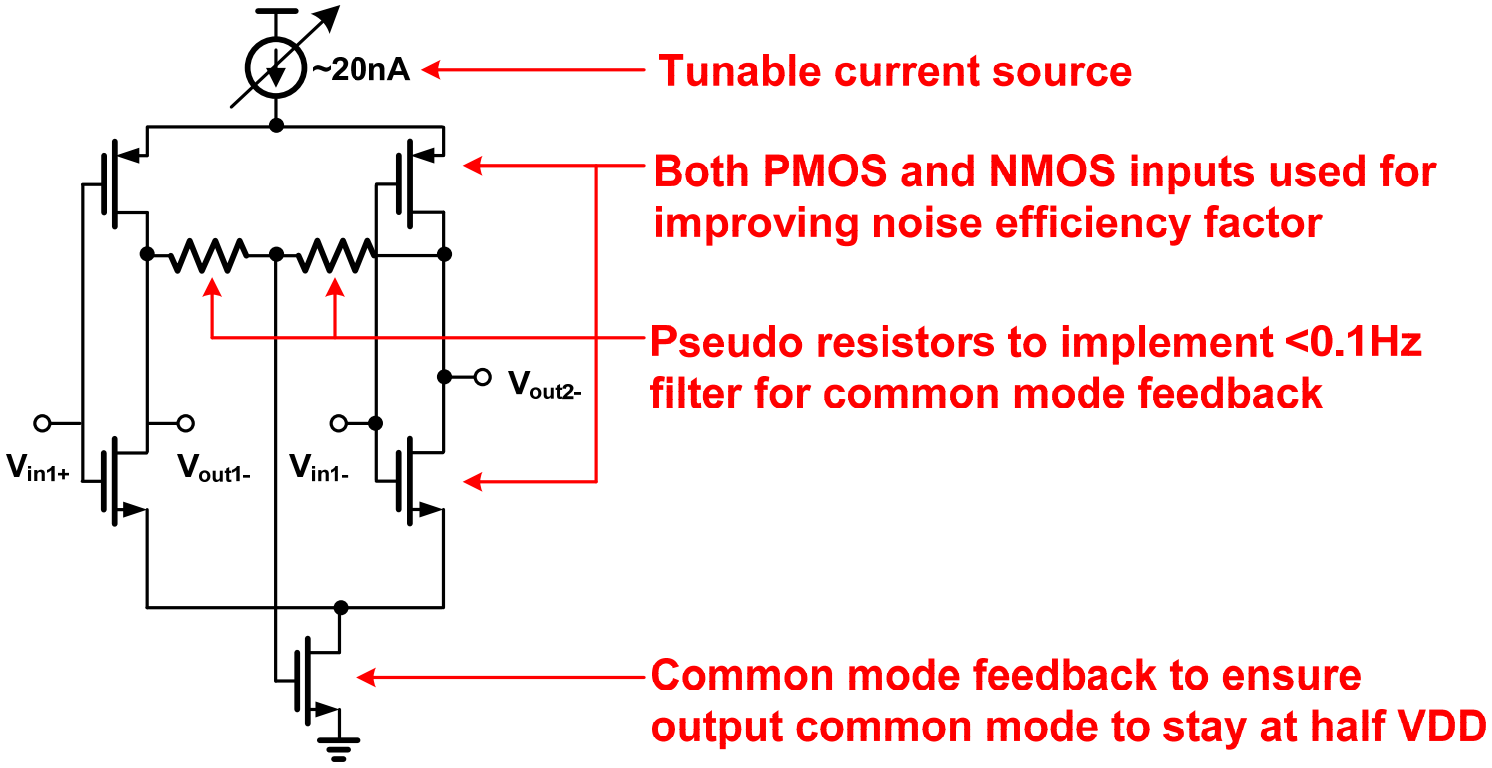




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Low Noise Amplifier

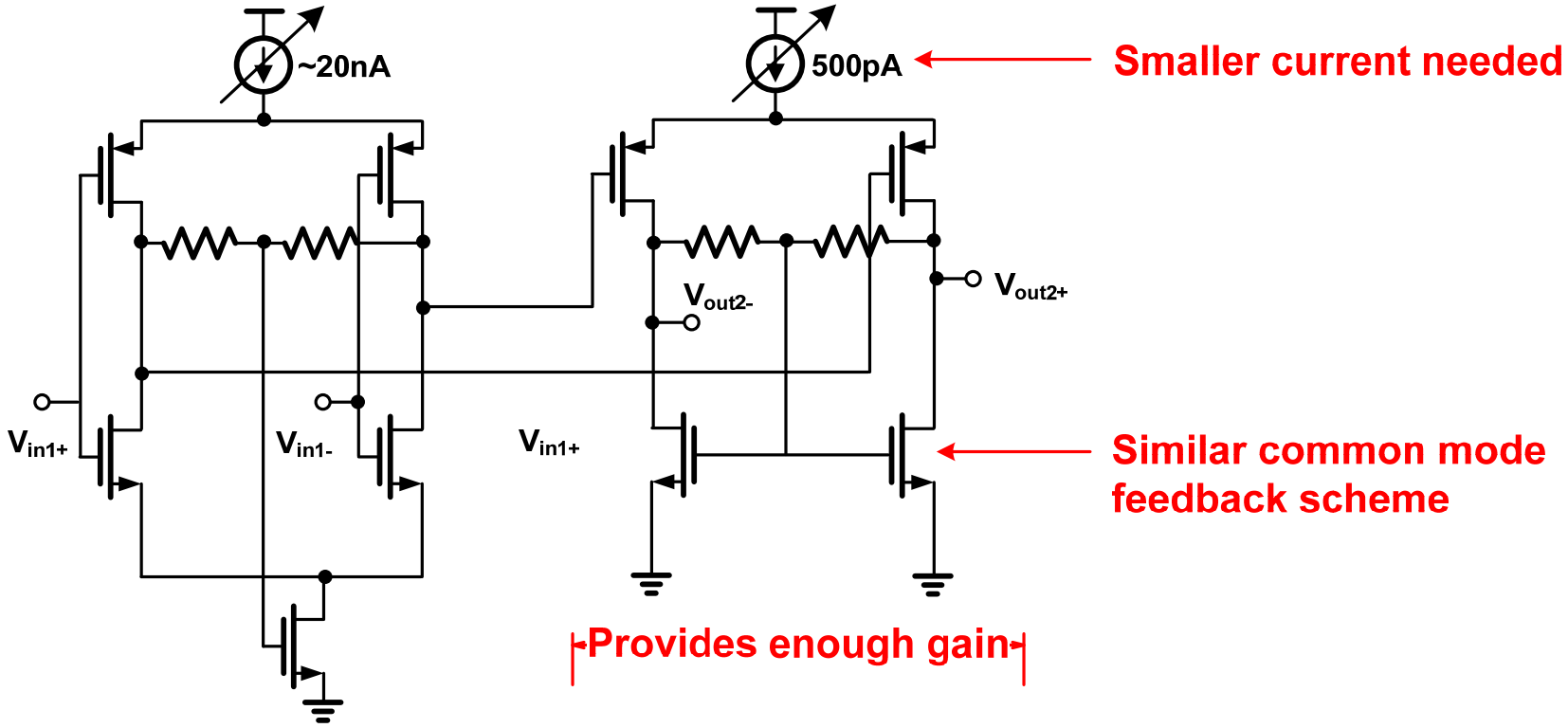
- 1st stage of amplifier



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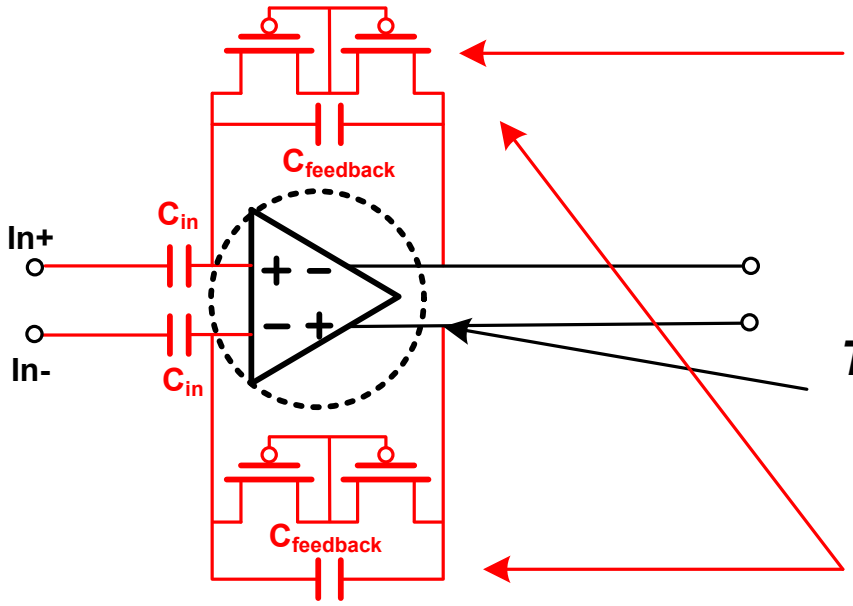
Low Noise Amplifier

- 2nd stage of amplifier



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LNA Feedbacks (1)



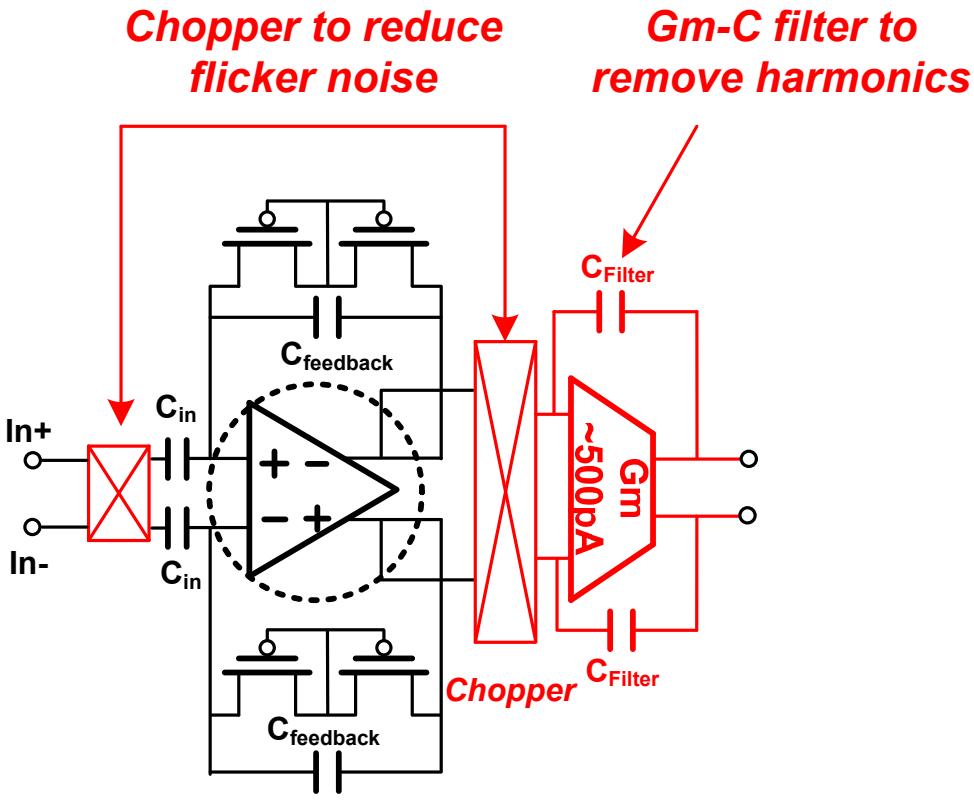
Pseudo resistor to generate <0.5Hz high pass corner

The Two Stage Amplifier in Previous Slide

Feedback to define fixed 50dB Gain

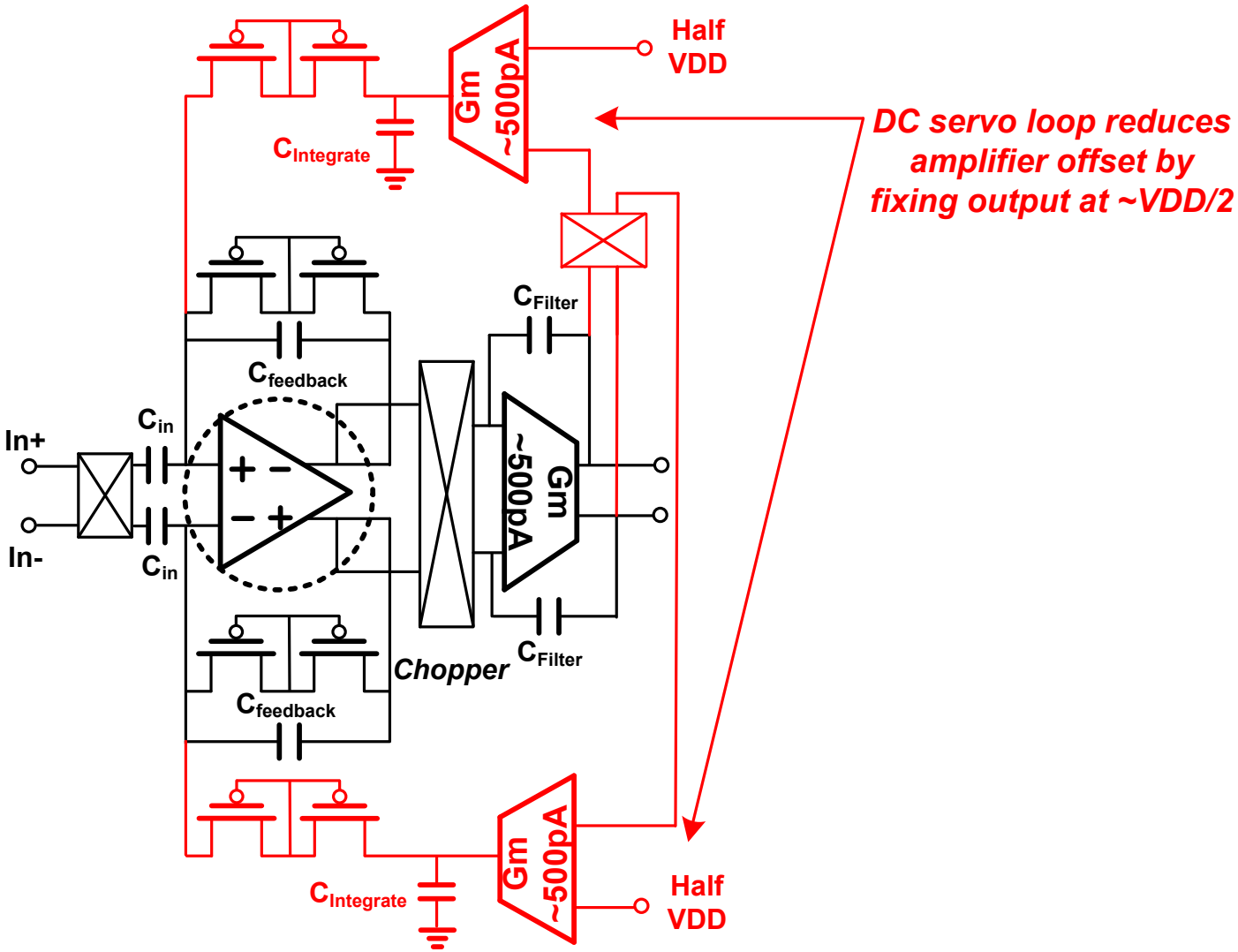
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LNA Feedbacks (2)



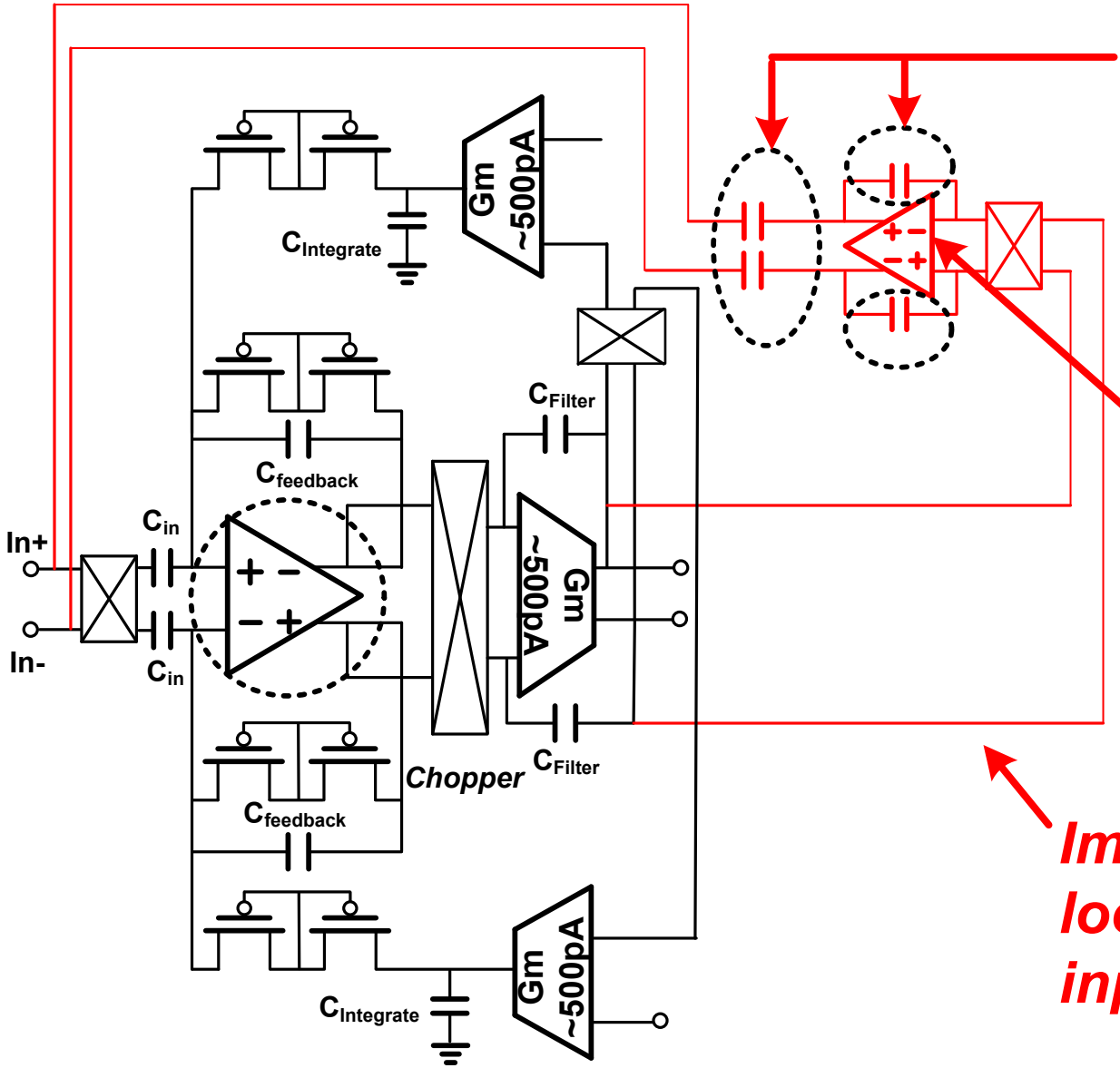
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LNA Feedbacks (3)



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LNA Feedbacks (4)



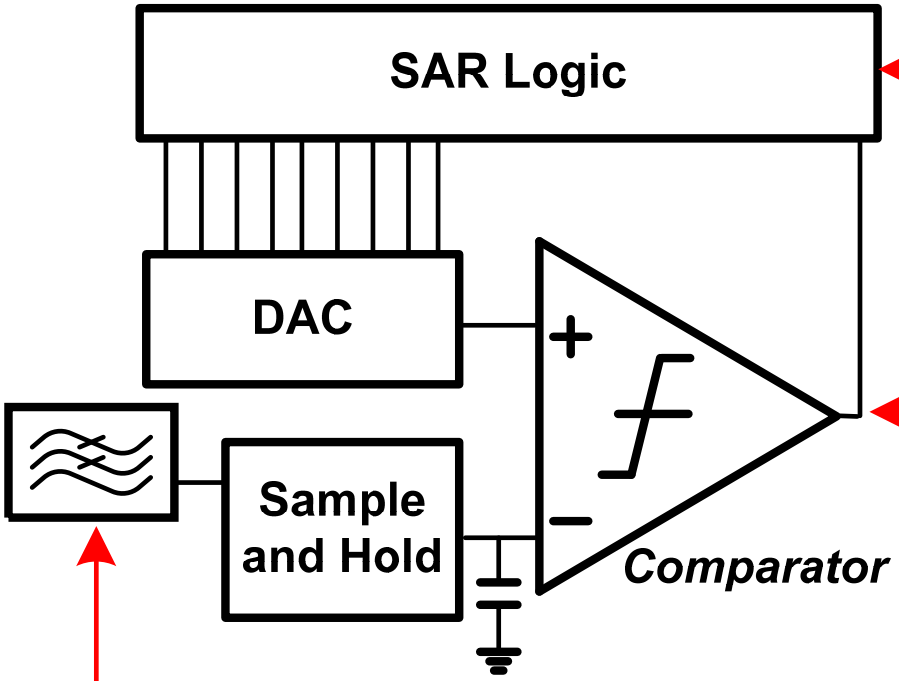
Use the same ratio as $C_{feedback}/C_{in}$ to generate the current

500pA Amplifier same as second stage of the core

Impedance boosting loop to increase input impedance

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SAR ADC



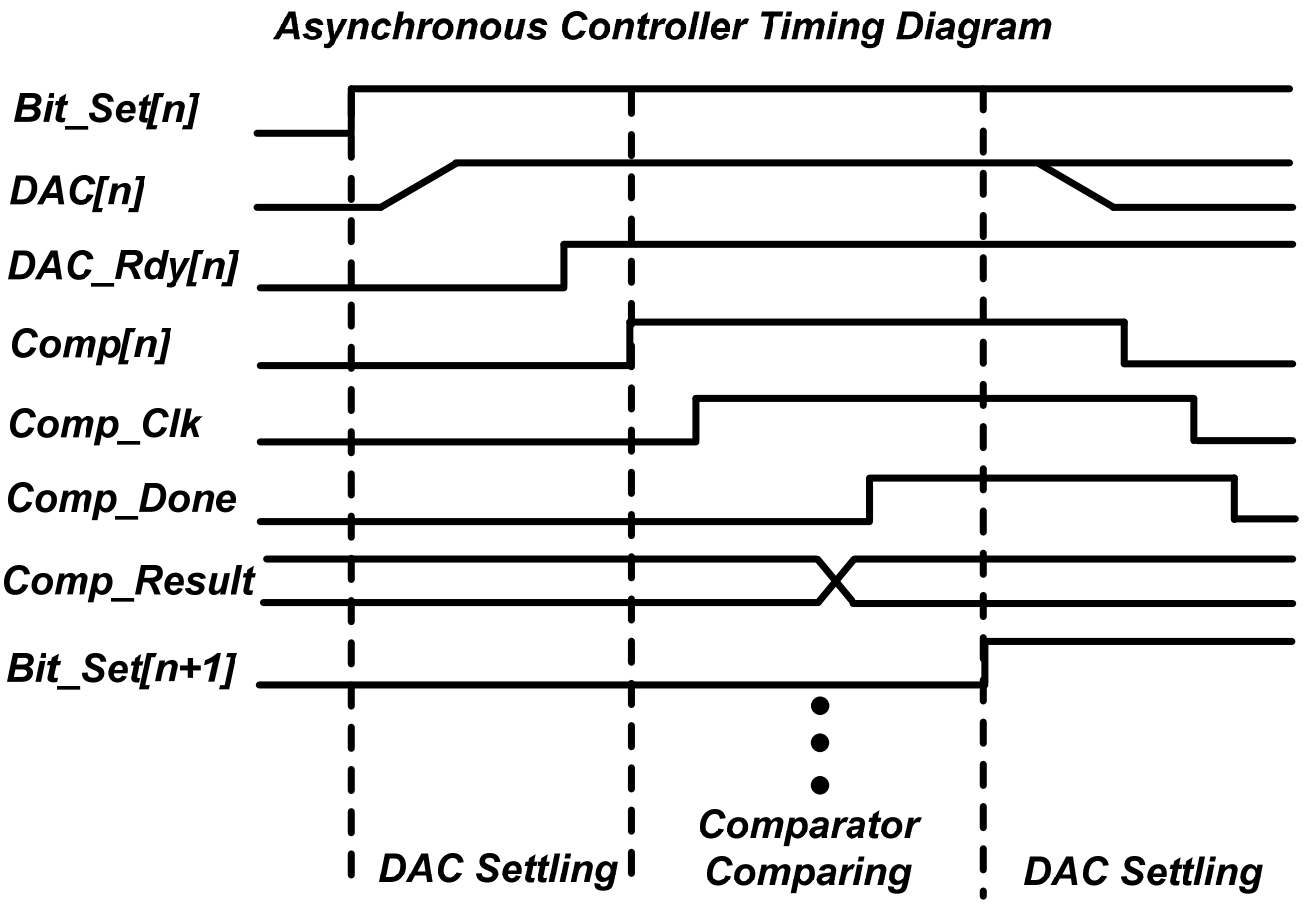
Asynchronous logic to reduce power consumption

One stage and split-footer design to reduce power

250Hz anti-aliasing Gm-C filter by 500pA amplfier

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SAR ADC



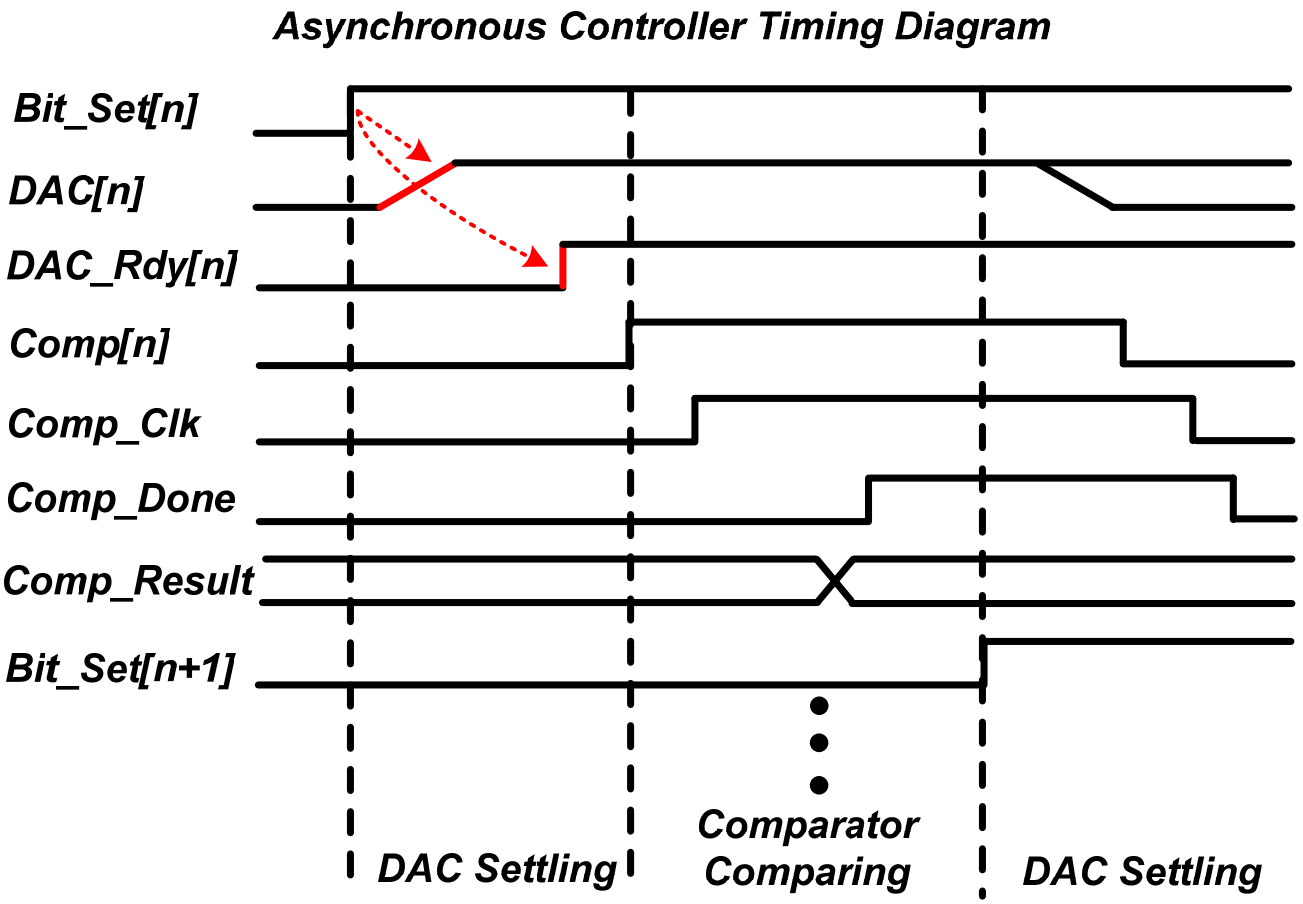
Comp_Clk: Connected to Footer of Clocked Comparator

Comp_Done: Pulled Up when Comparison is Finished

Comp_Result: Latched(SR Latch) Result of Comparator Output

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SAR ADC



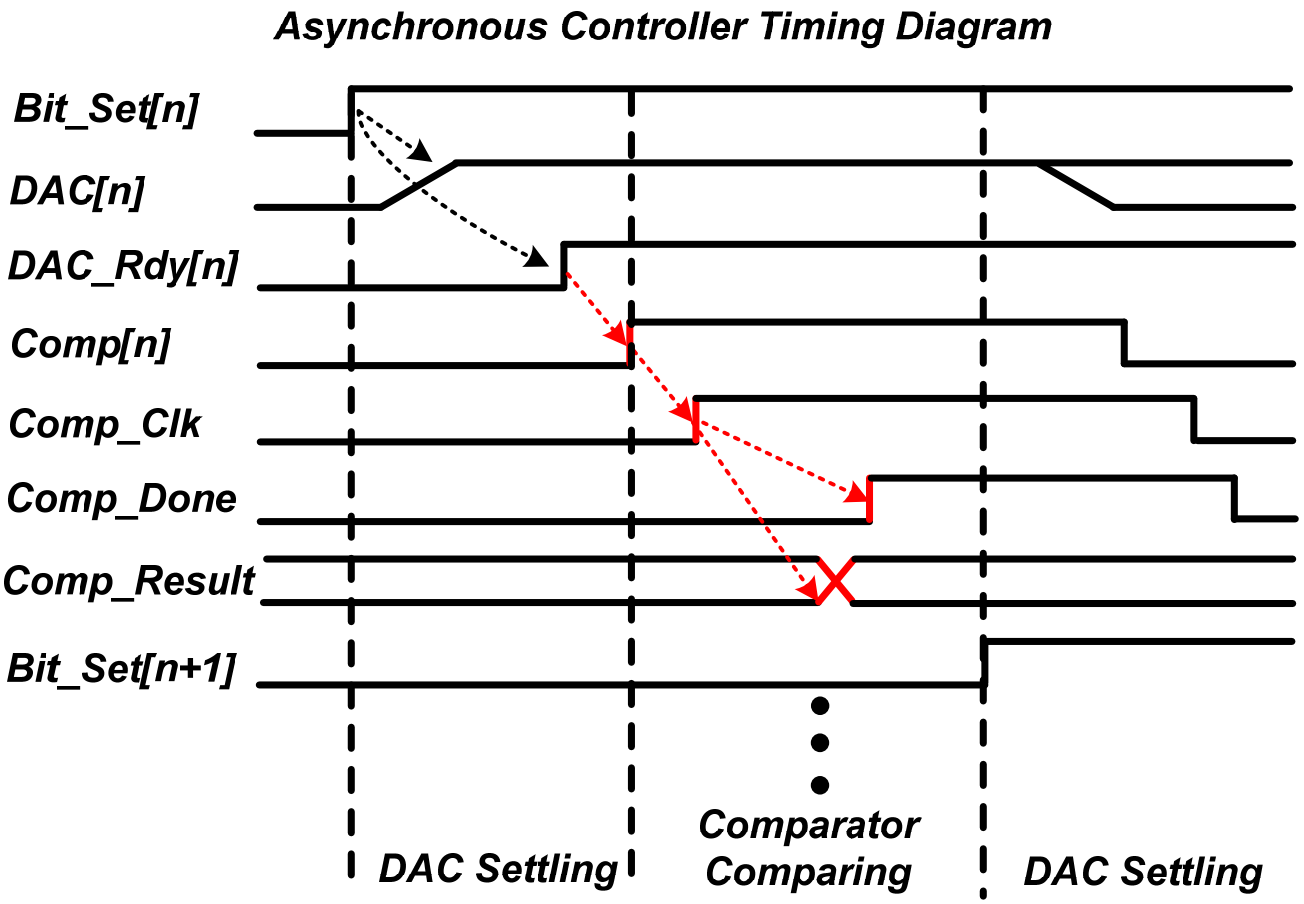
Comp_Clk: Connected to Footer of Clocked Comparator

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SAR ADC



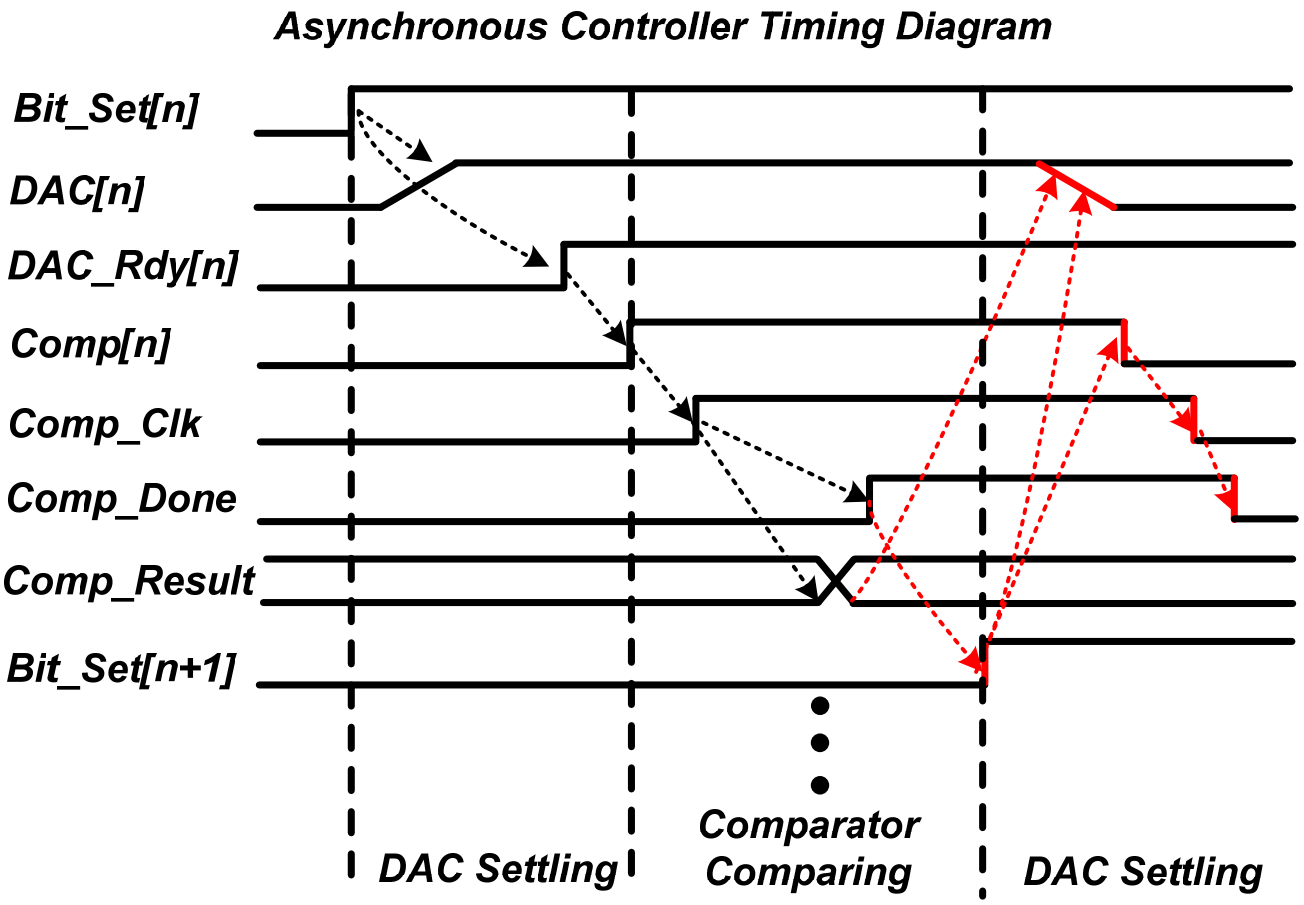
Comp_Clk: Connected to Footer of Clocked Comparator

Comp_Done: Pulled Up when Comparison is Finished

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SAR ADC



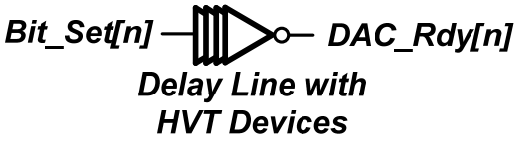
Comp_Clk: Connected to Footer of Clocked Comparator

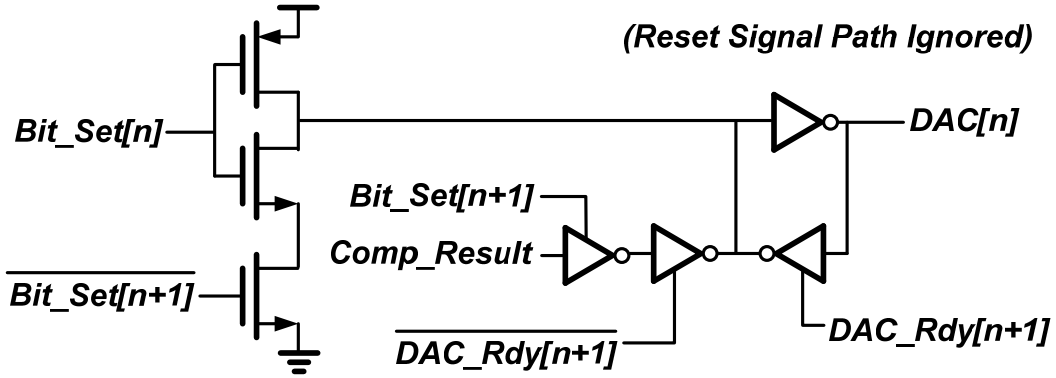
Comp_Done: Pulled Up when Comparison is Finished

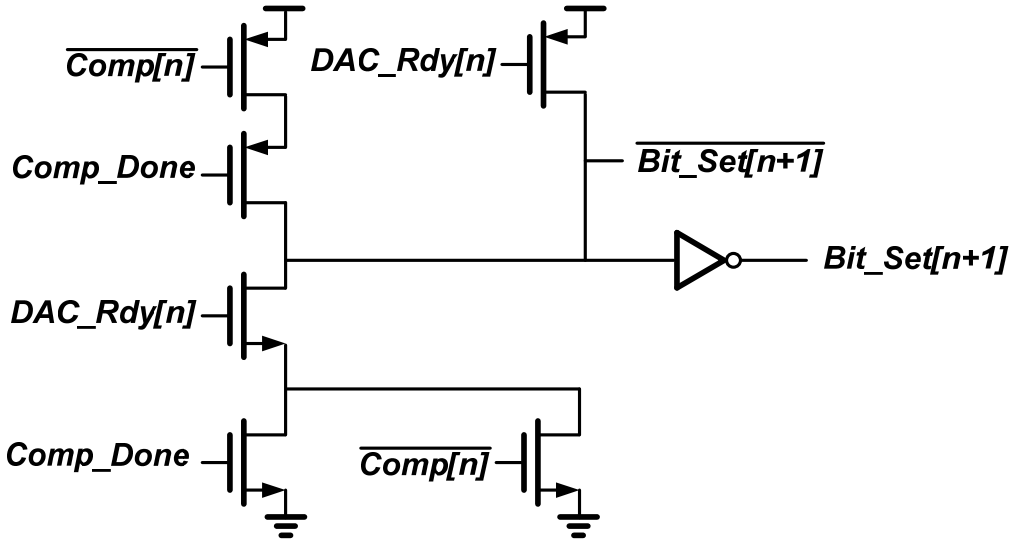
Comp_Result: Latched(SR Latch) Result of Comparator Output

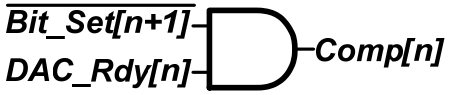
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SAR ADC



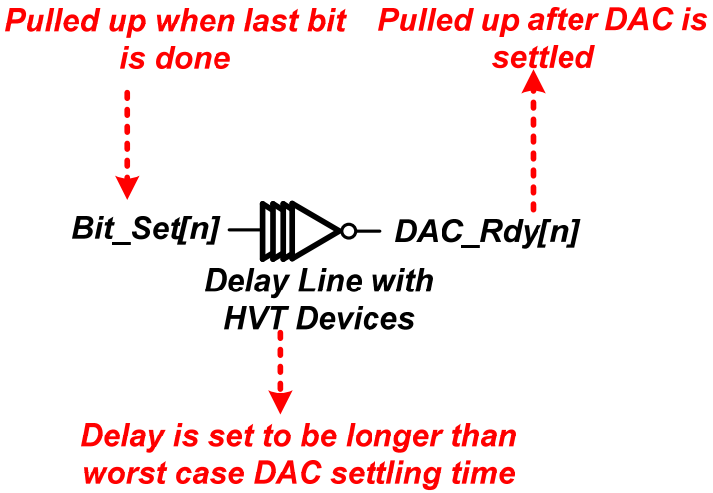






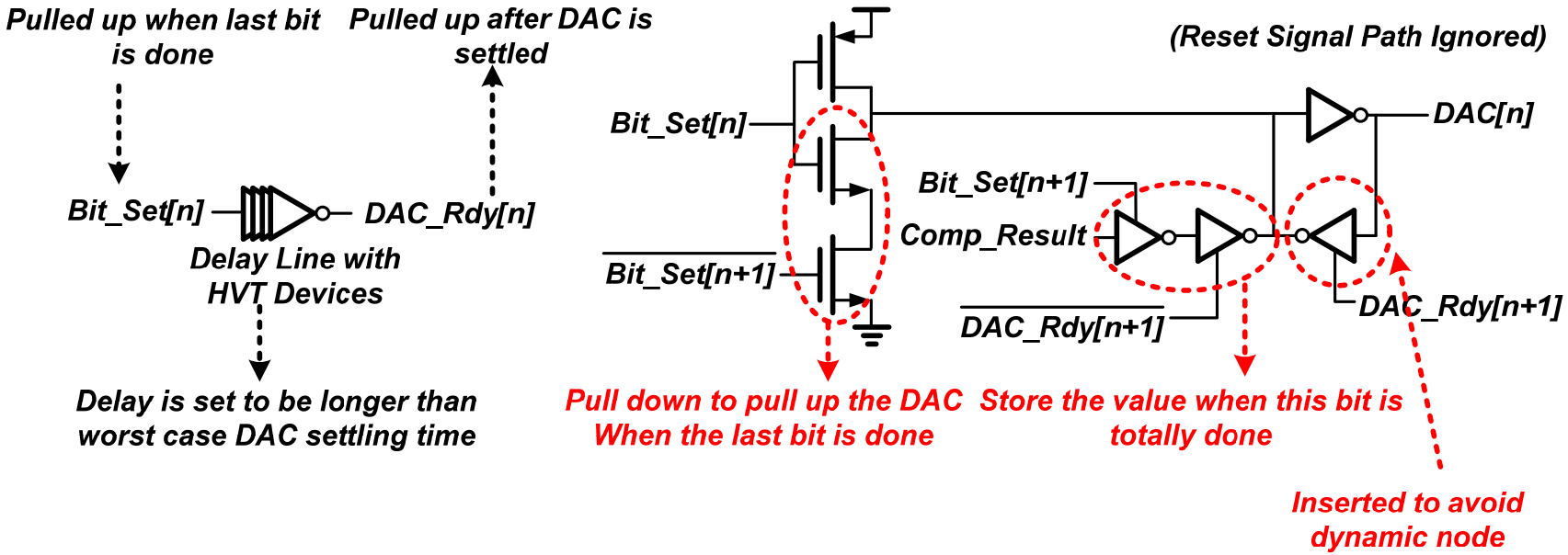
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SAR ADC



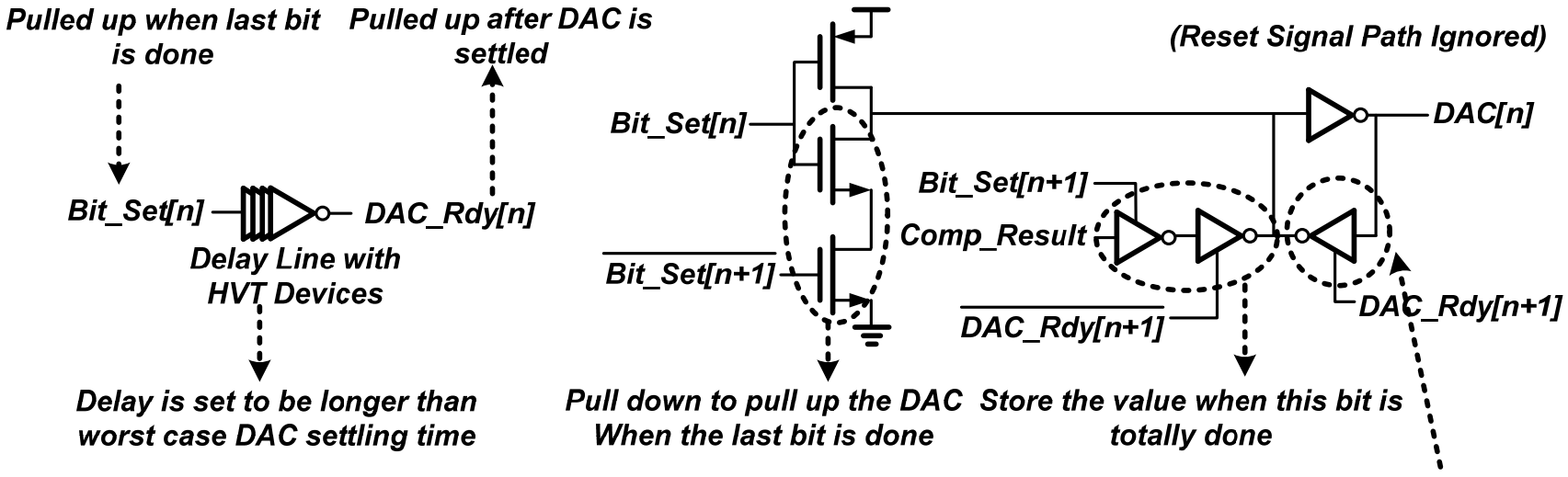
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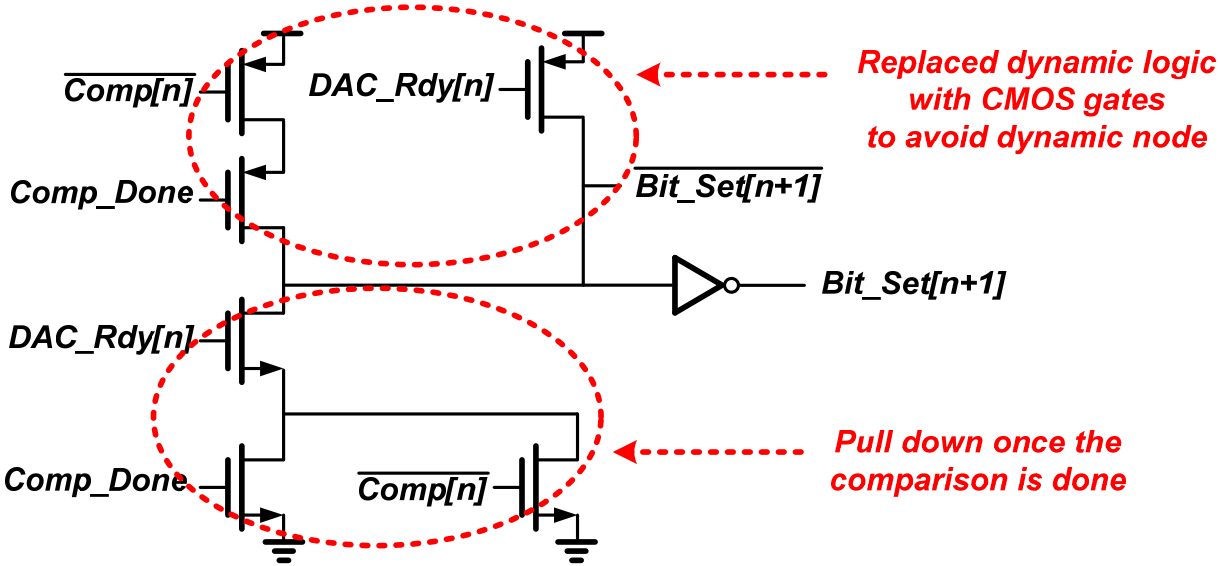
SAR ADC



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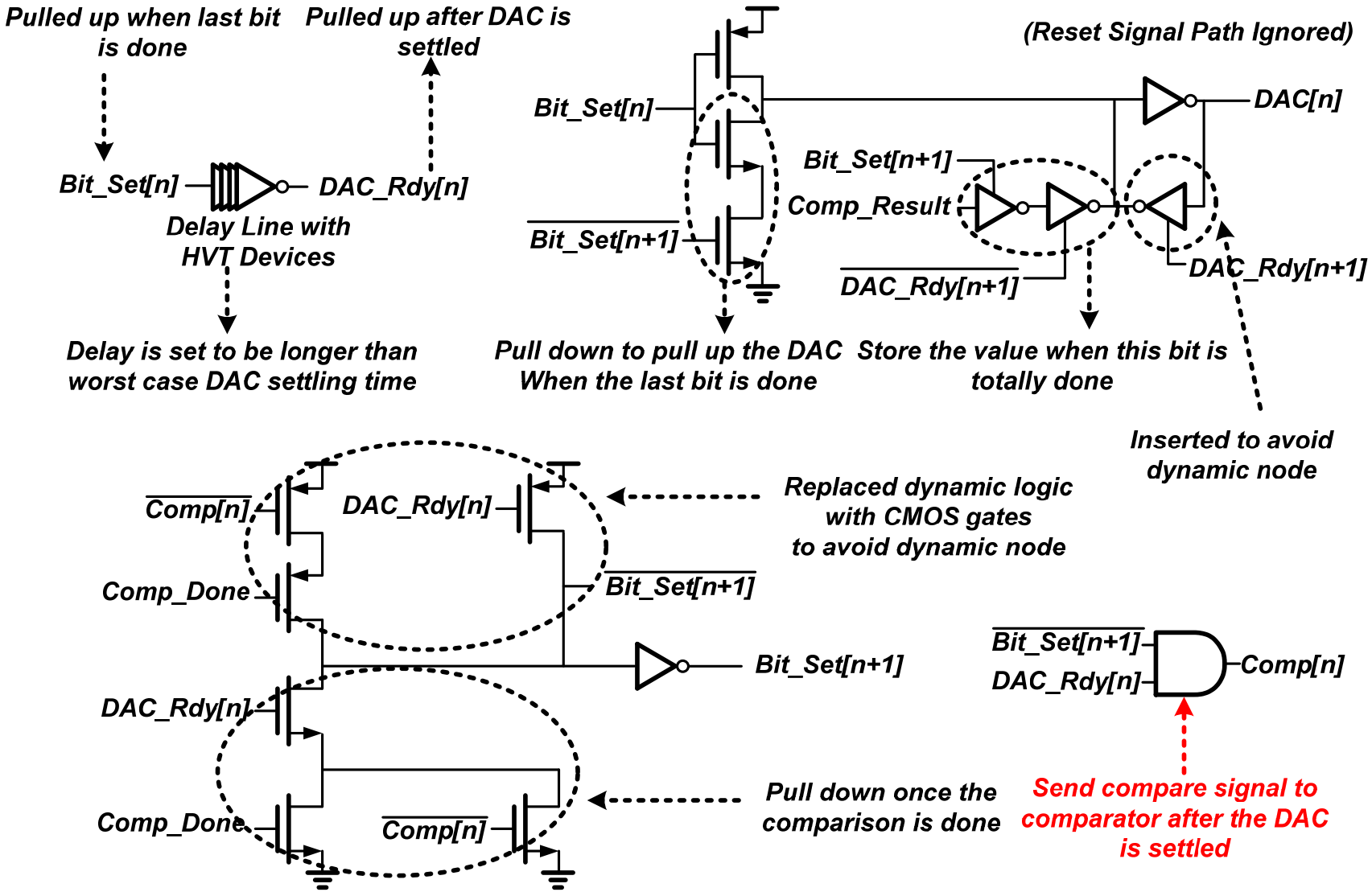
SAR ADC





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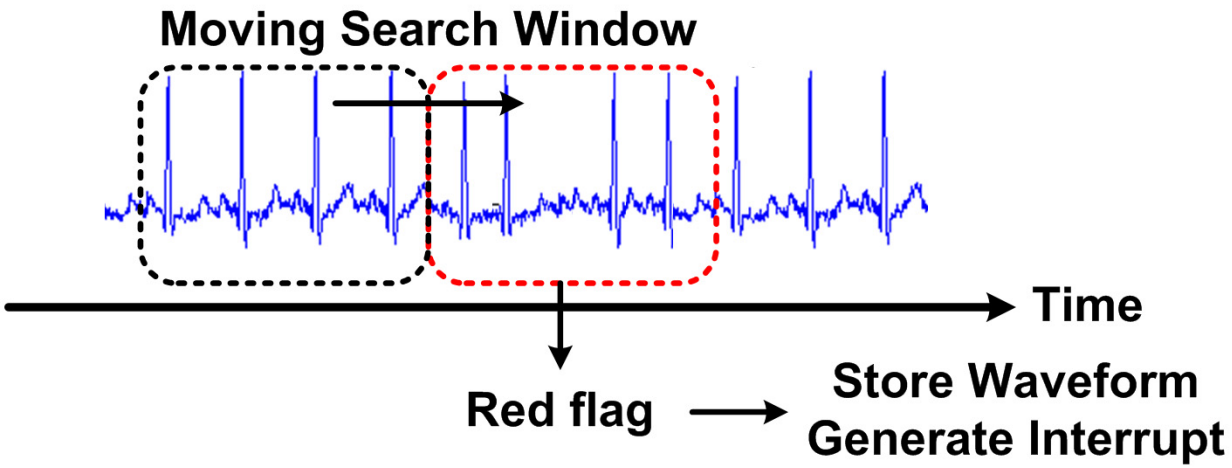
SAR ADC



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Arrhythmia Detection

- Continuous search in shifting 10-sec window

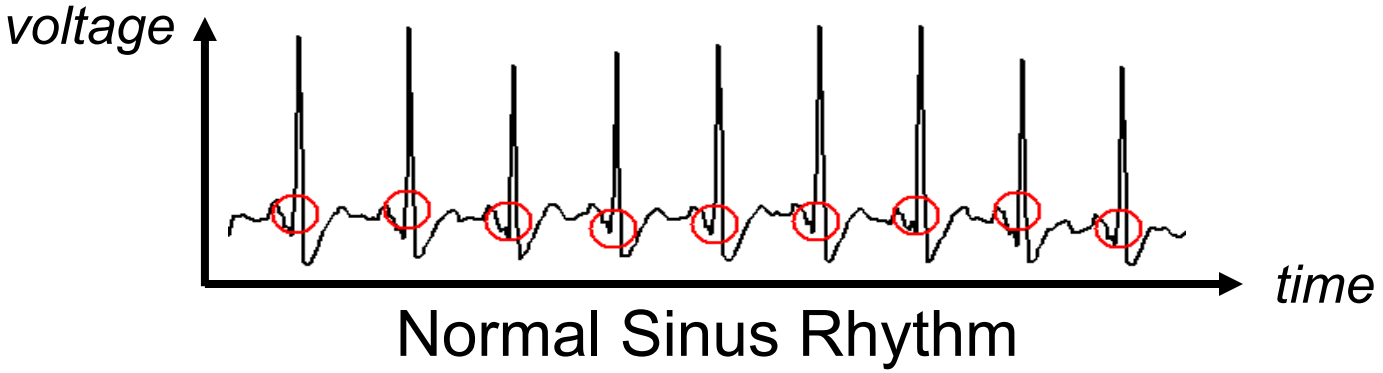


- Search for irregular rhythm or rate
 1. Peak detection
 2. Frequency spectrum analysis

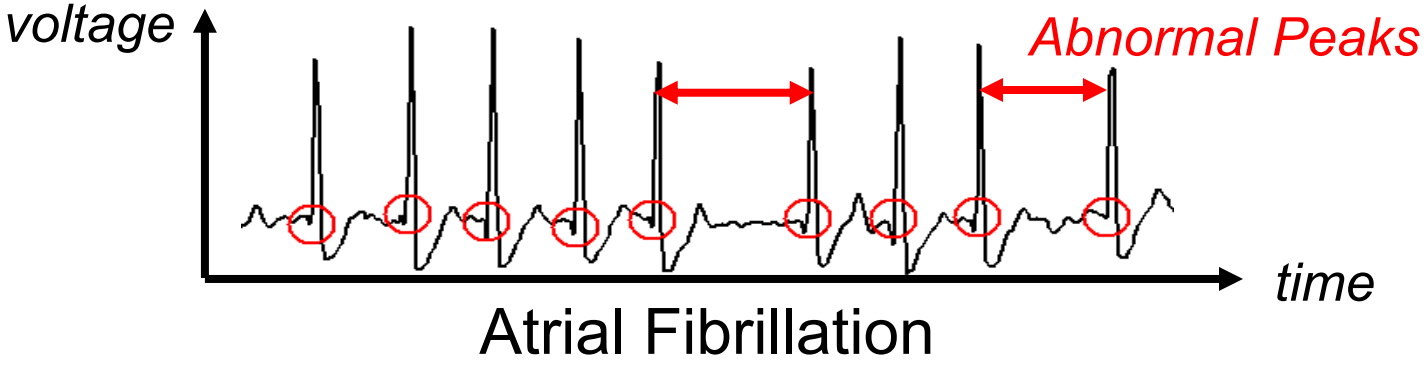
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Detection Algorithms (1)

- Time domain detection
 - Detect QRS peaks
 - Calculate peak-to-peak distances
 - Use variance(σ^2) for thresholding



Normal Sinus Rhythm

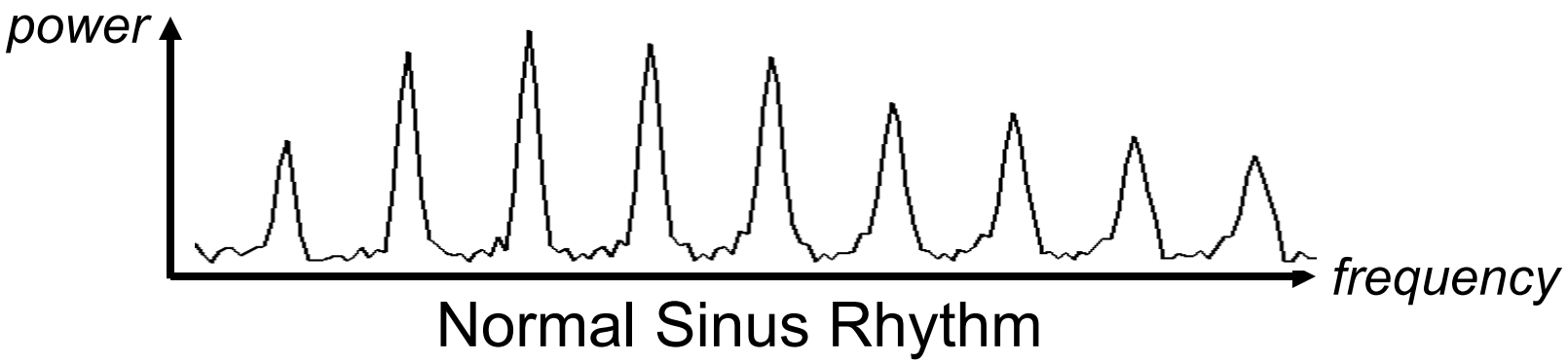


Atrial Fibrillation

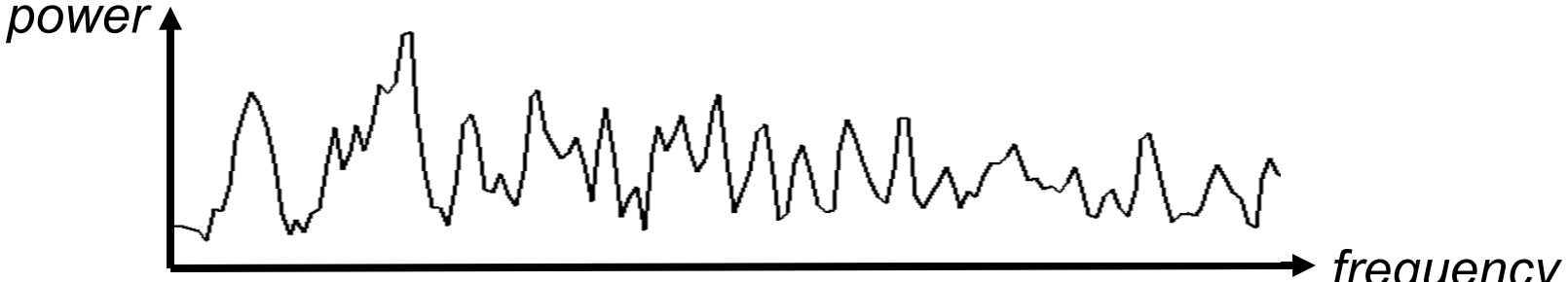
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Detection Algorithms (2)

- Frequency domain detection
 - Directly analyze frequency spectrum
 - Normal rhythm → clear peaks in spectrum
 - Abnormal rhythm → vague or no peak in spectrum



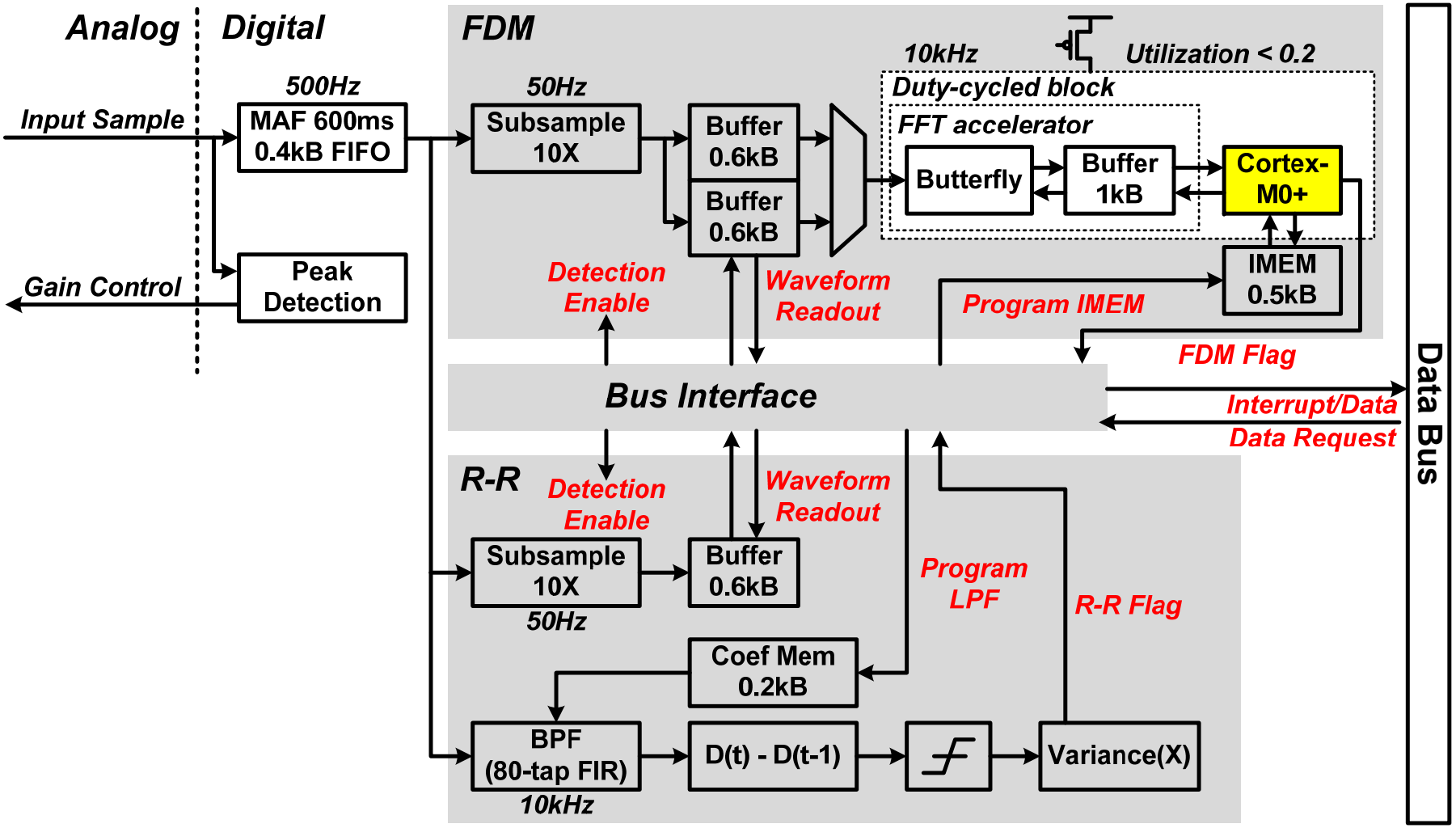
Normal Sinus Rhythm



Atrial Fibrillation

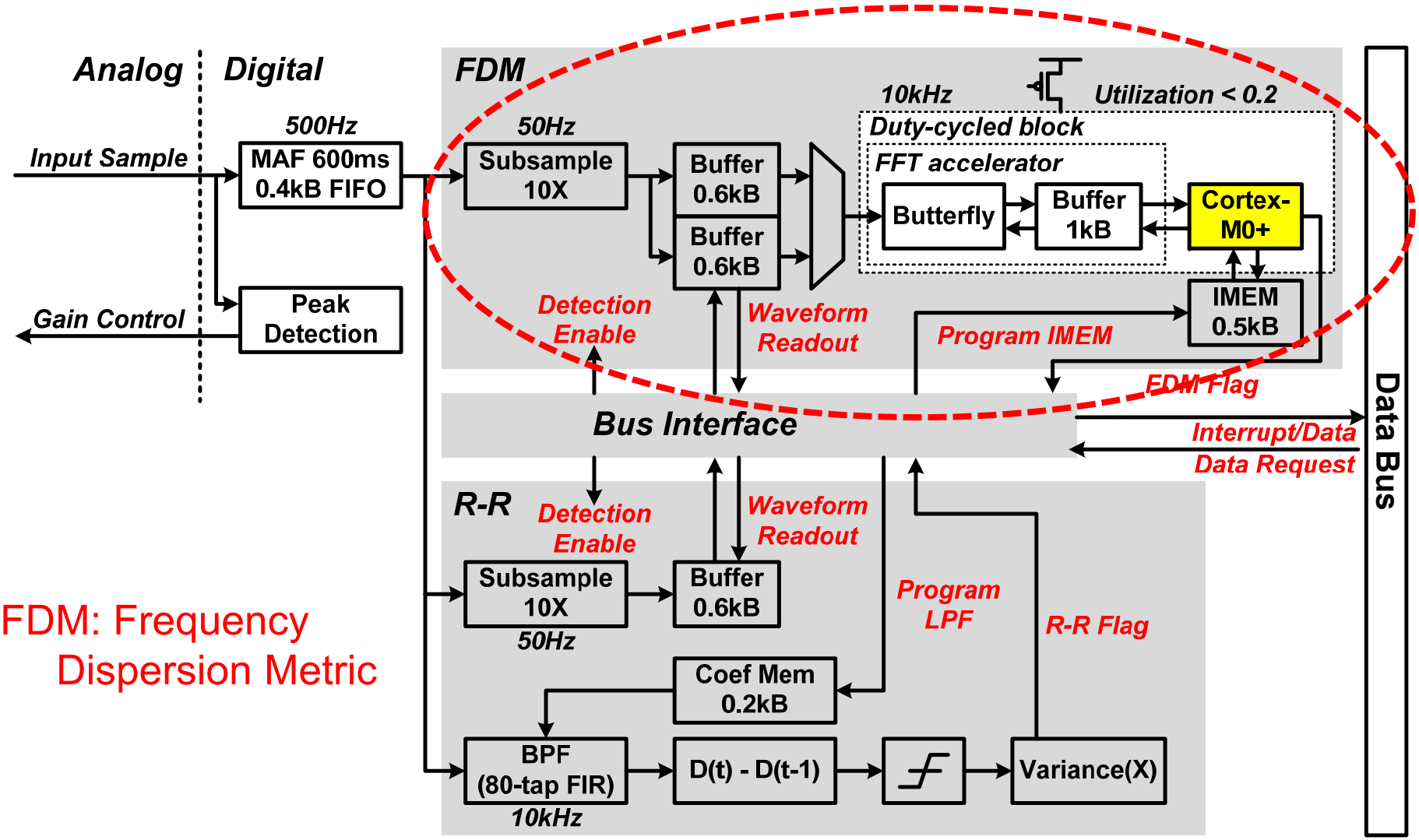
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Digital Back End



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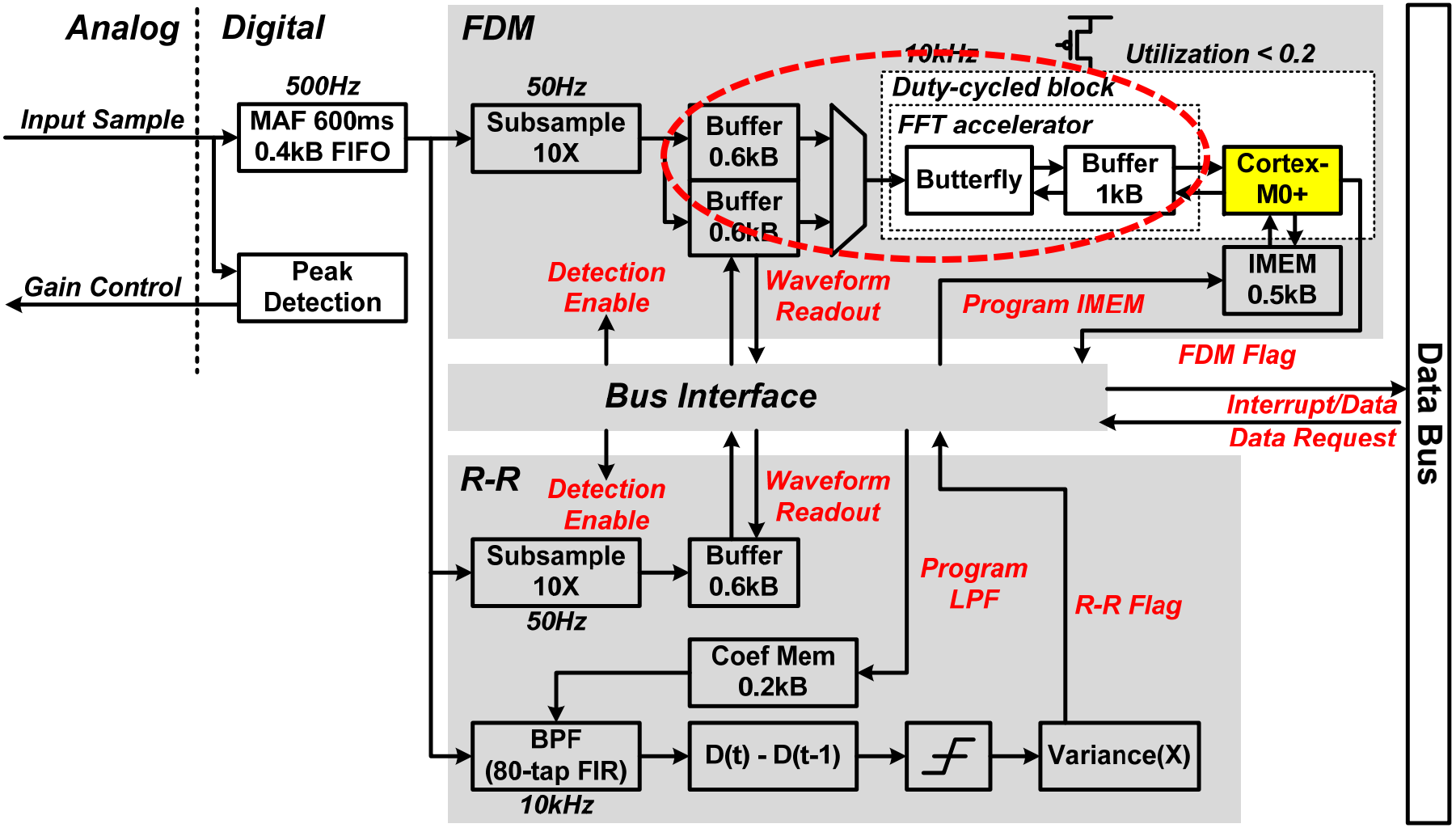
FDM Block



FDM: Frequency Dispersion Metric

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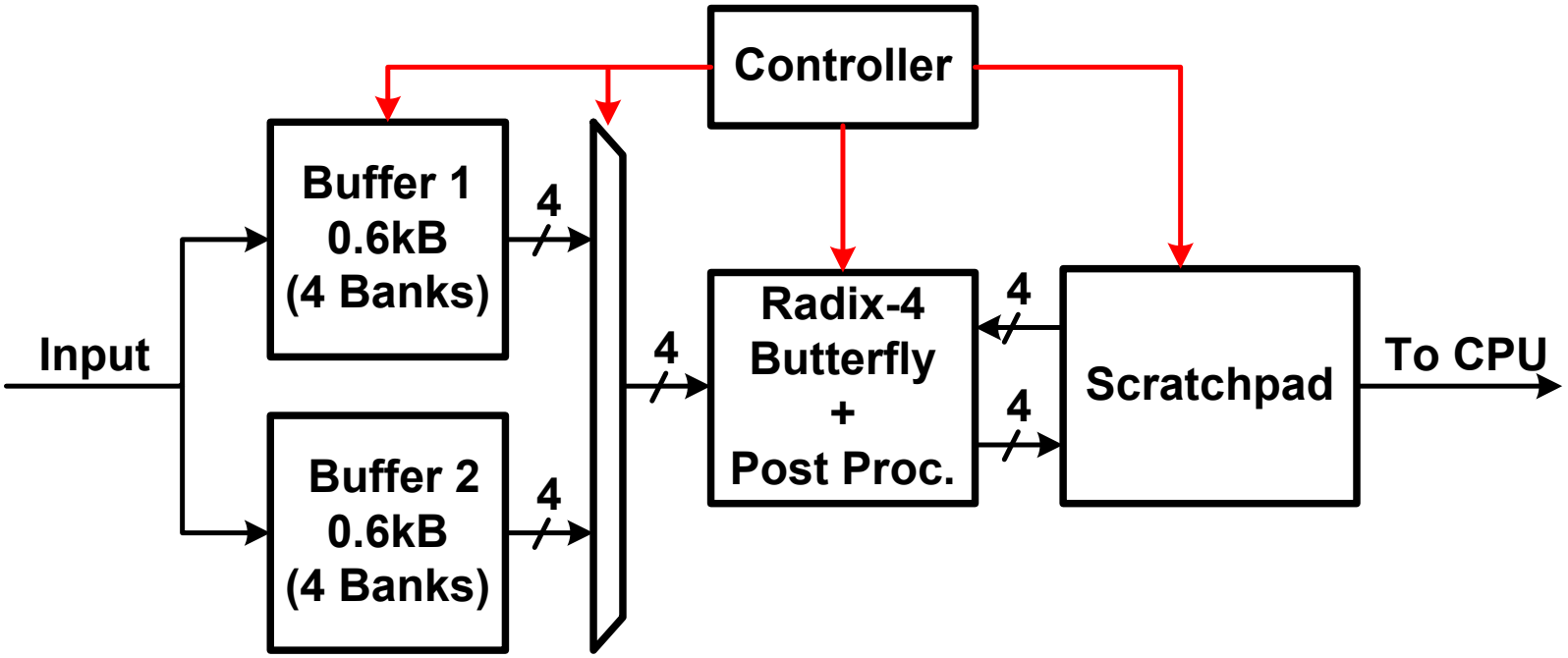
FFT Accelerator



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FFT Accelerator

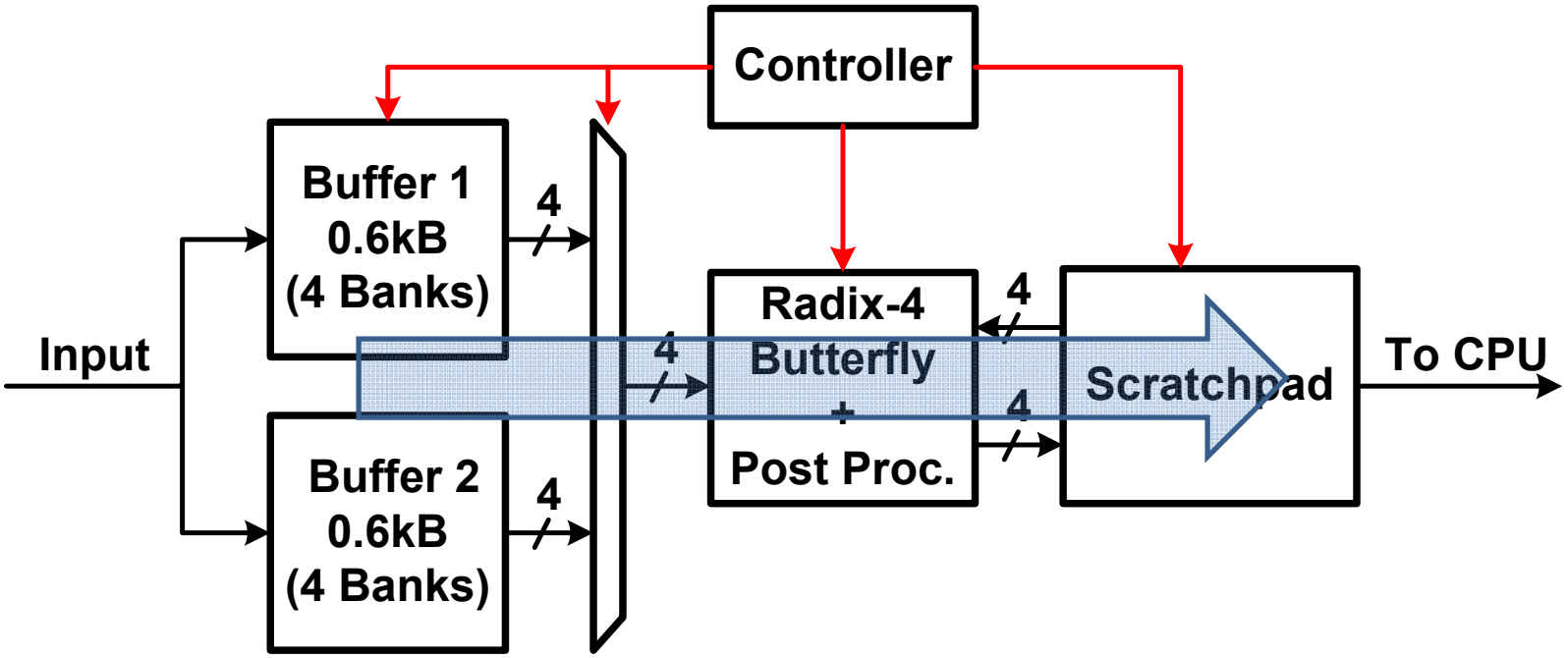
- 512-point real-valued FFT
 - 256-pt complex-valued + post-processing step
 - Radix-4 butterfly
 - Ping-pong buffer for continuous monitoring



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FFT Accelerator

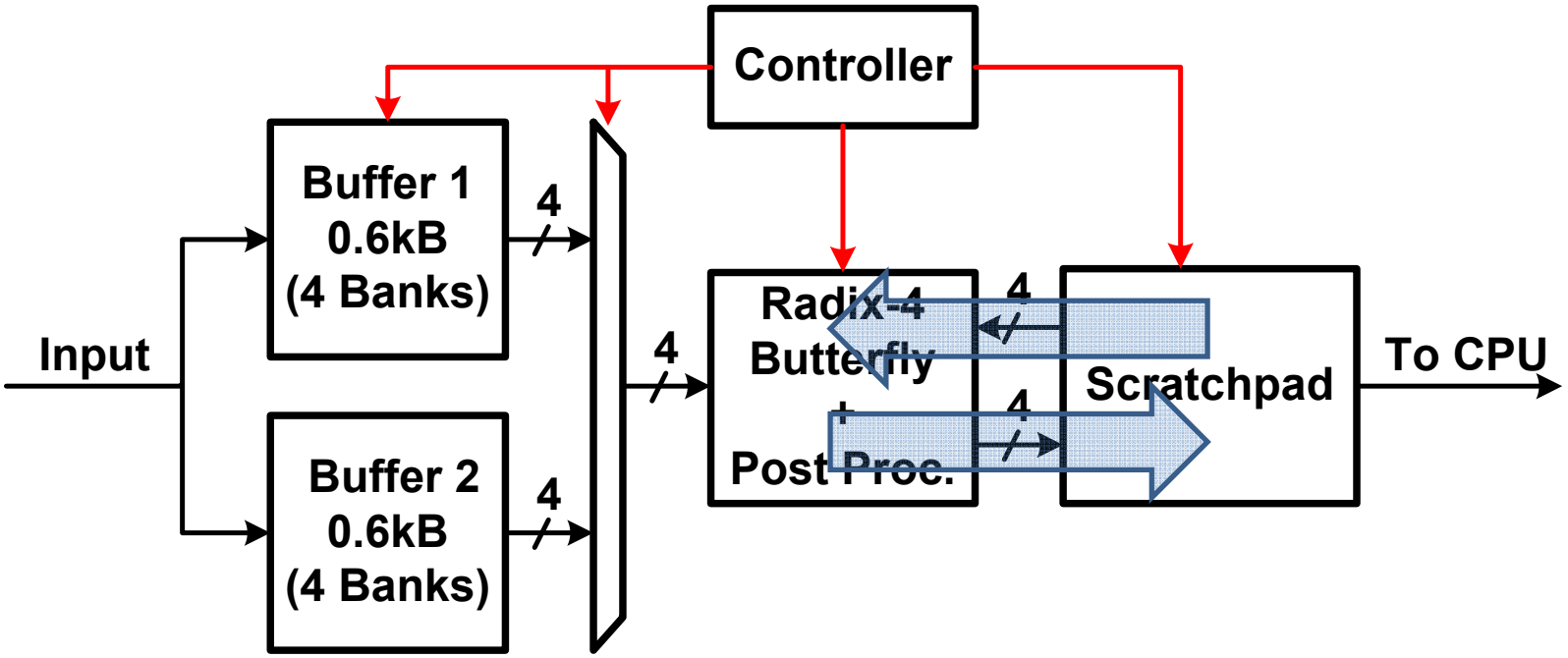
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 - Ping-pong buffer for continuous monitoring



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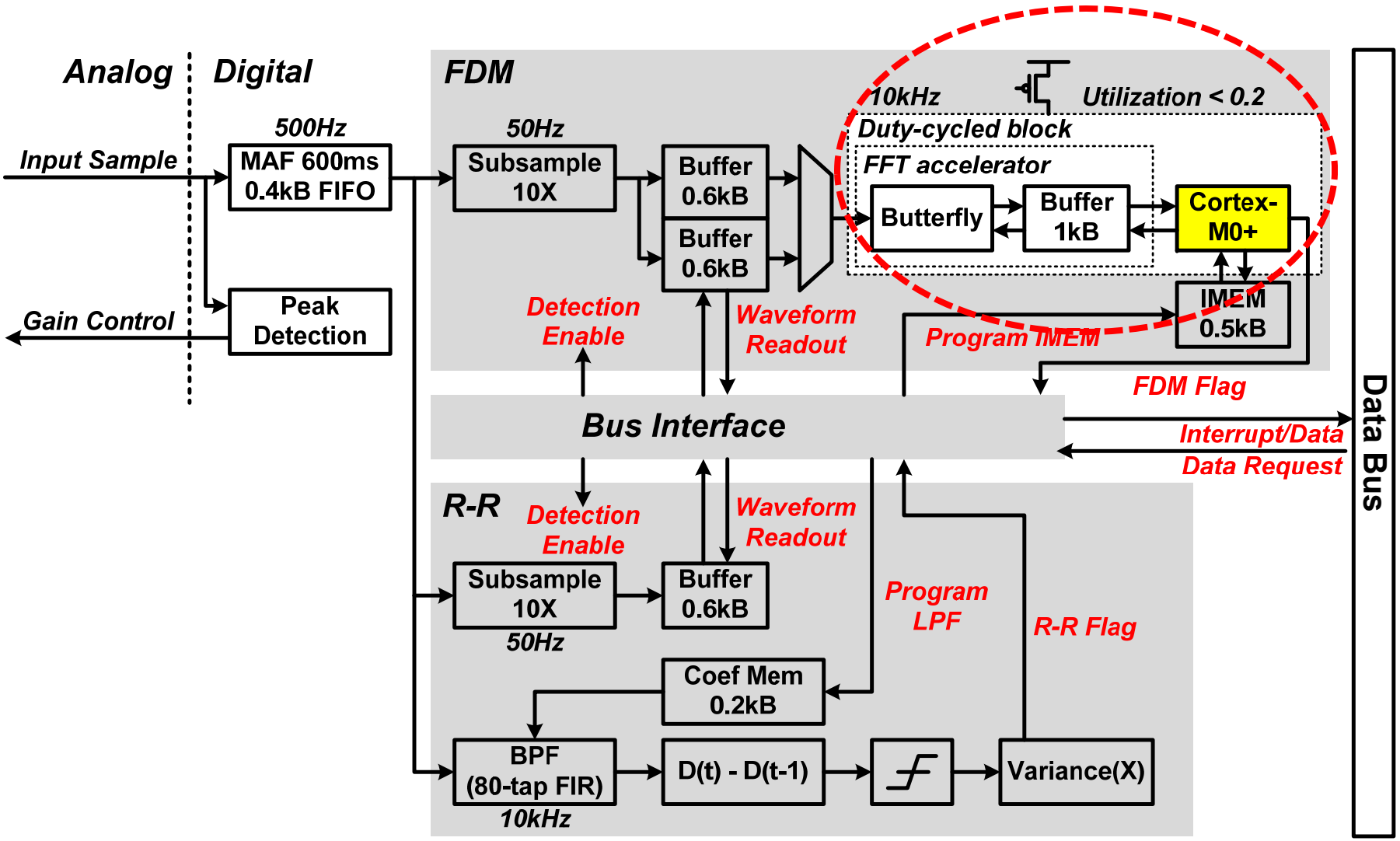
FFT Accelerator

- 512-point real-valued FFT
 - 256-pt complex-valued + post-processing step
 - Radix-4 butterfly
 - Ping-pong buffer for continuous monitoring



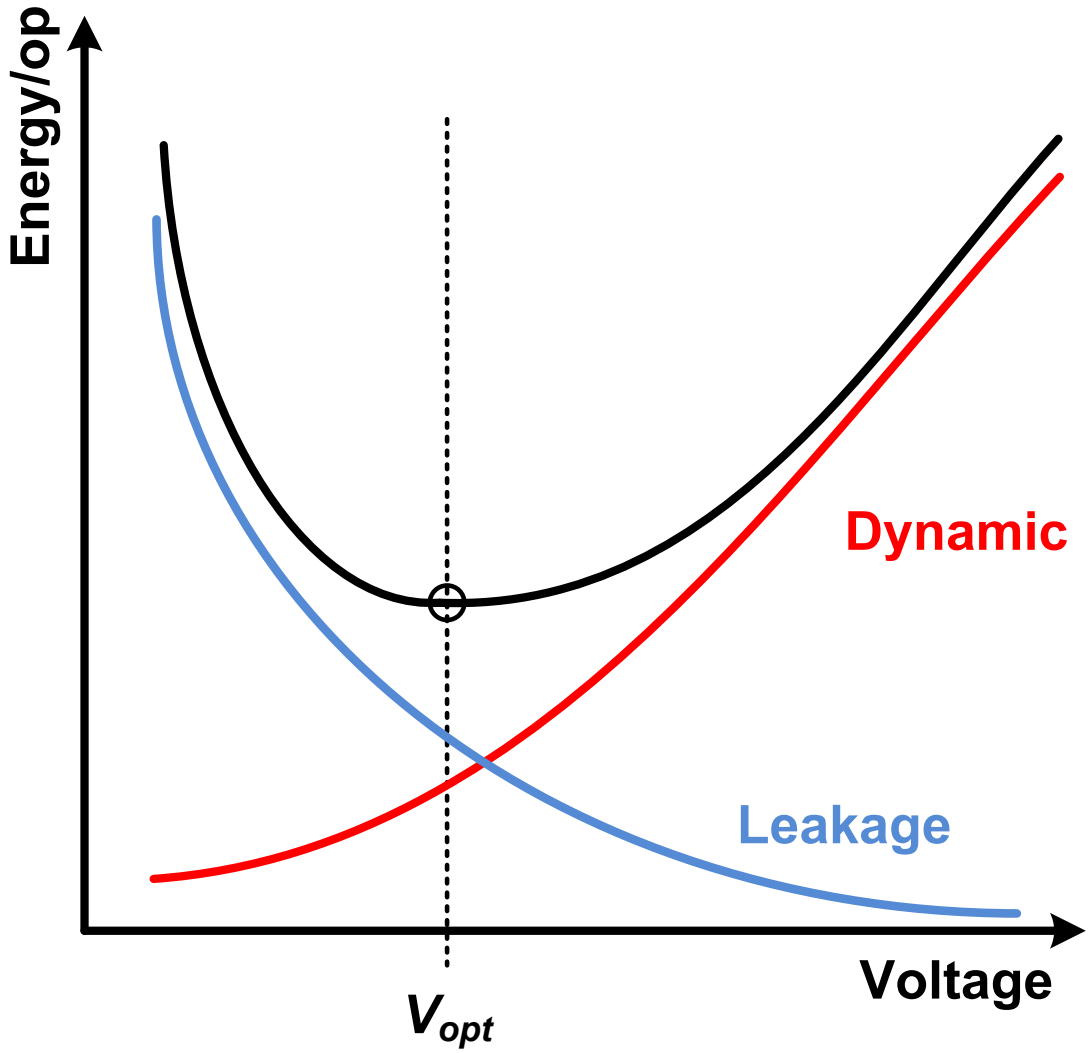
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Minimum Energy Computation



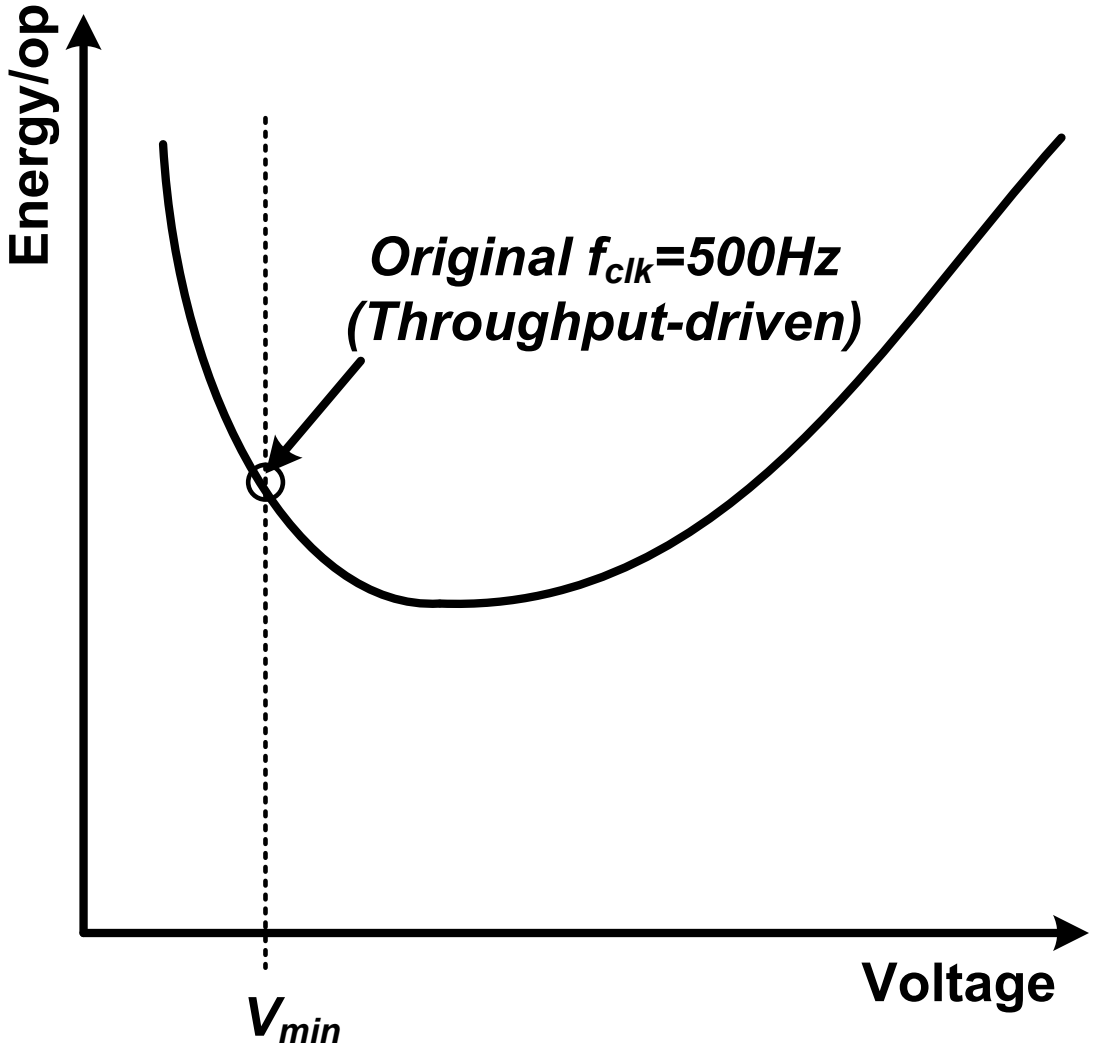
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Minimum Energy Computation



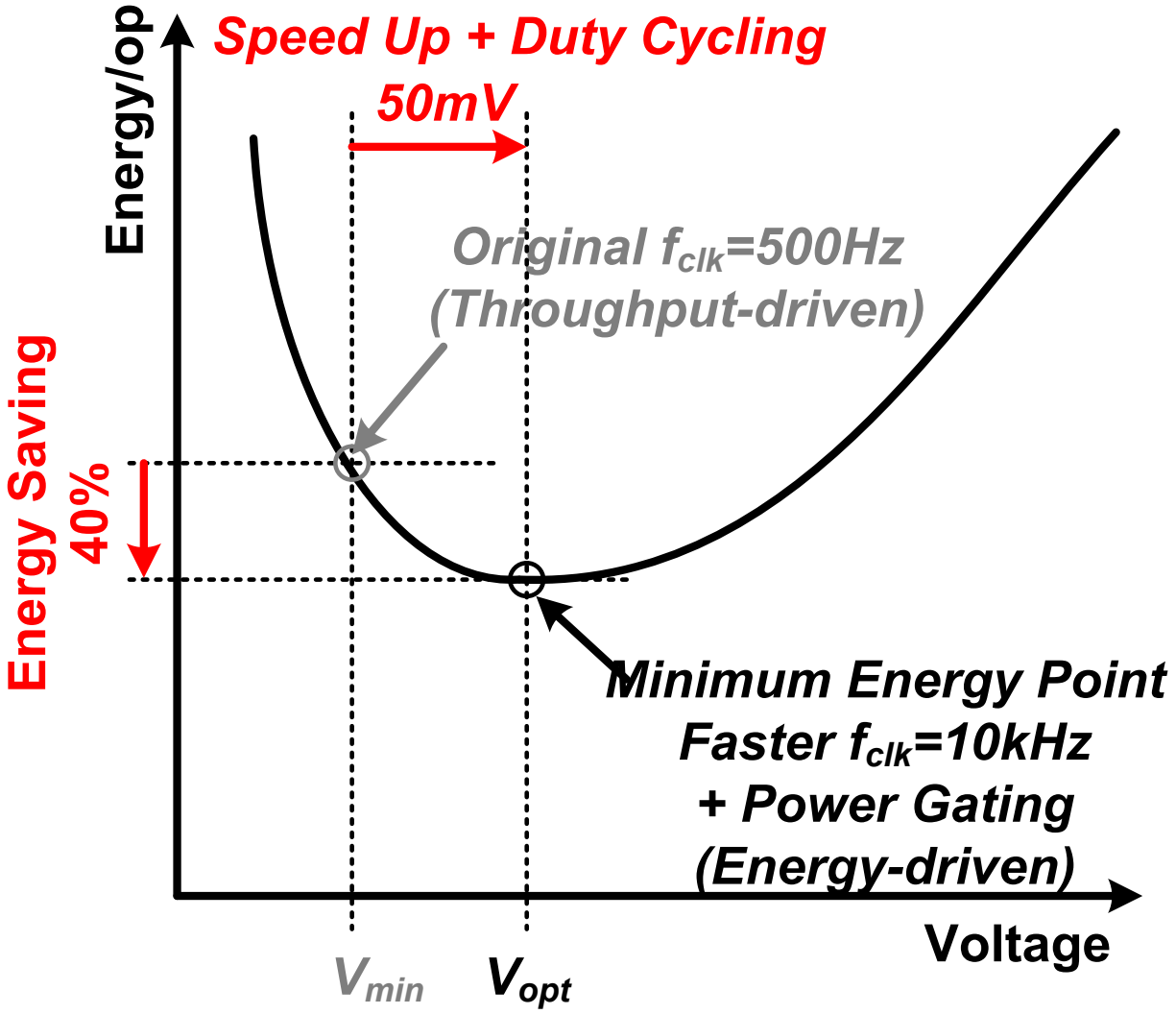
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Minimum Energy Computation



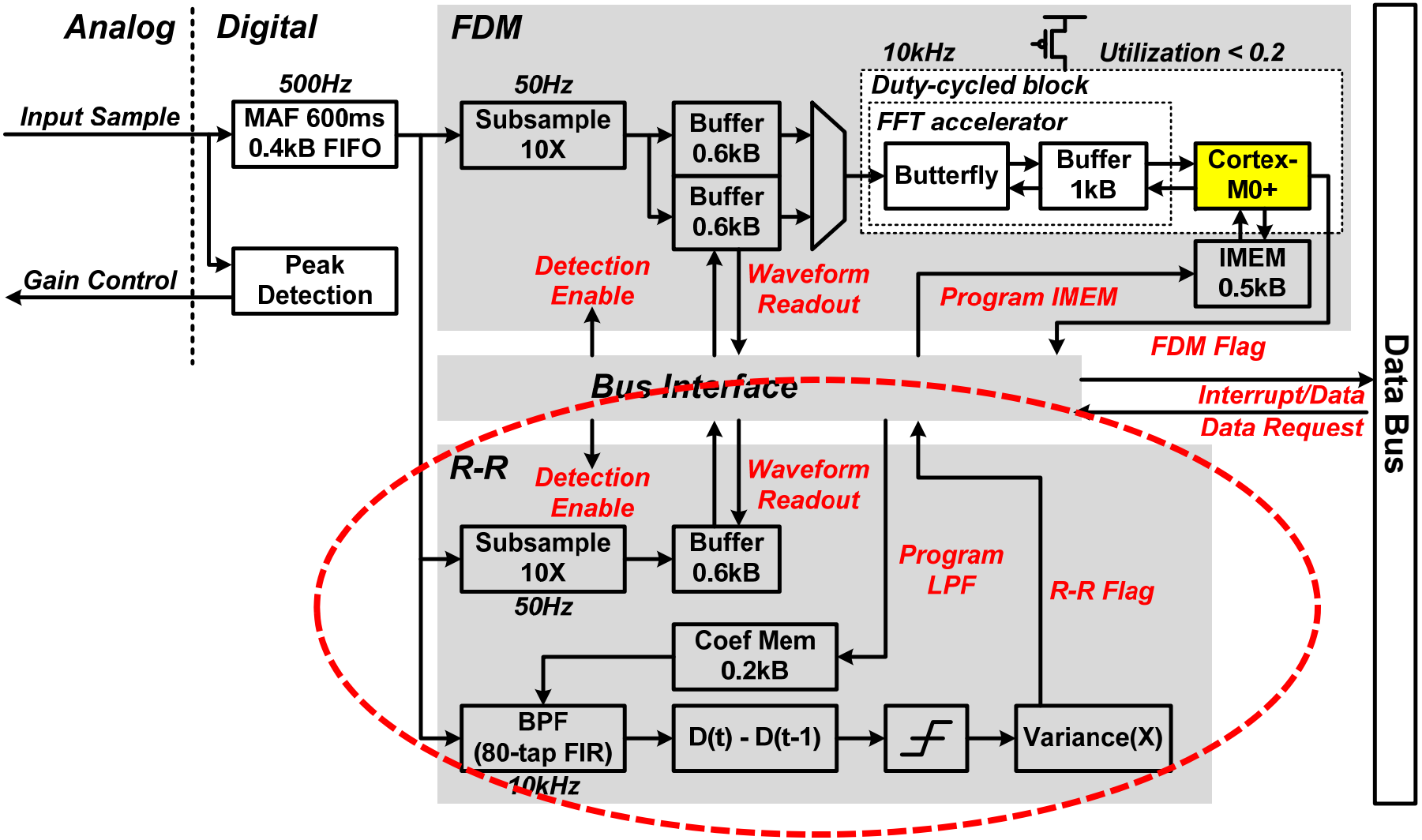
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Minimum Energy Computation



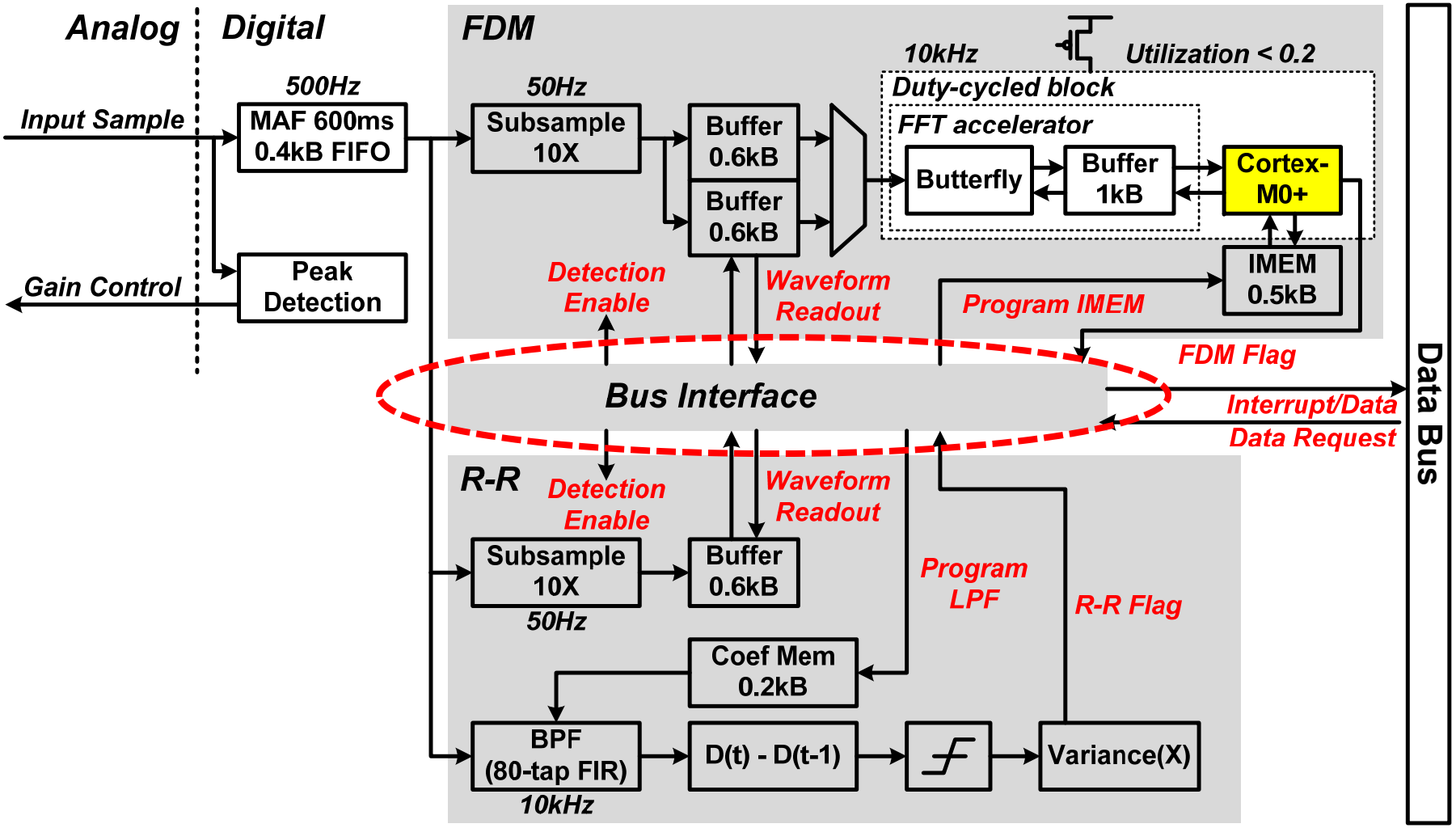
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R-R Block



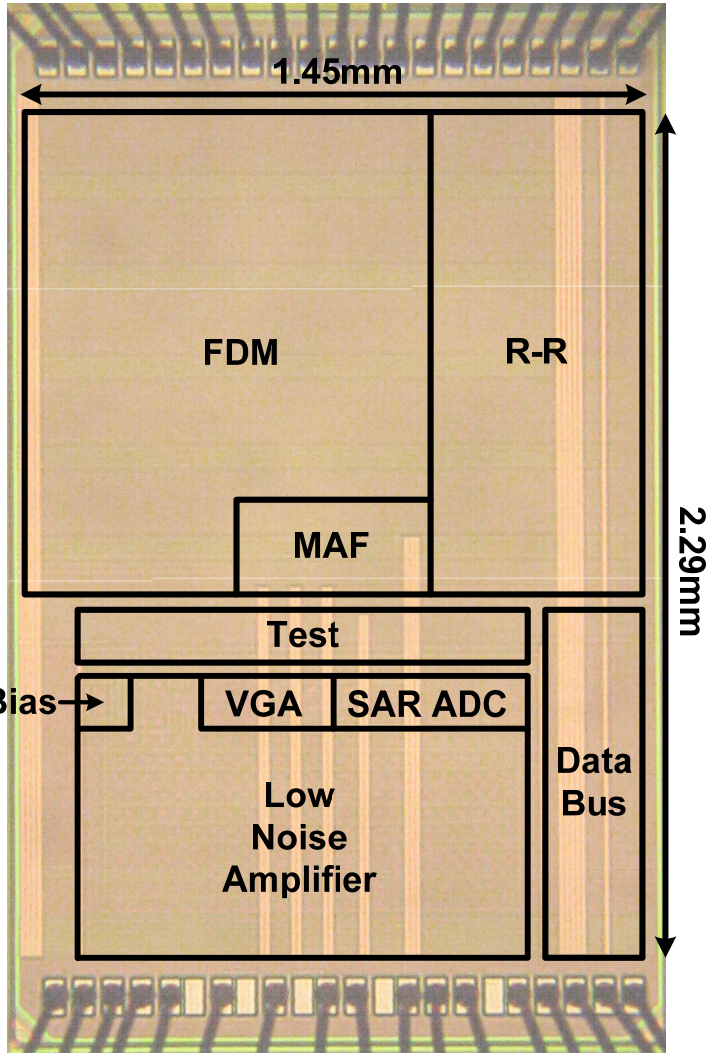
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Bus Interface



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Chip Microphotograph



Technology		65 nm
Die Area		1.45 × 2.29 mm^2
AFE	V_{DD}	0.6 V
	Current	28 nA (LNA + VGA) 3 nA (ADC)
	Gain	51 ~ 96 dB
	Bandwidth	250 Hz
	Input Impedance	> 10 MΩ
	Input Referred Noise	253 nV/$\sqrt{Hz}$ (Noise Floor) 6.52 μV (RMS)
	NEF	2.64
	NEF×VDD^2	0.95
	ADC Bits	8 Bits
	ADC Sampling Frequency	500 Hz
DSP	V_{DD}	0.4 V
	Clock Frequency	10 kHz
	Total Memory	3.7 kB
	Power Consumption	45 nW (FDM) 92 nW (R-R)
	Main Processing Units	ARM Cortex-M0+ 16-b 512-pt RV FFT 80-tap FIR

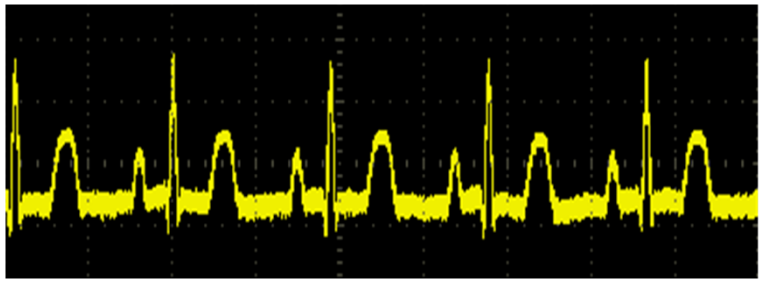
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Measurement Results

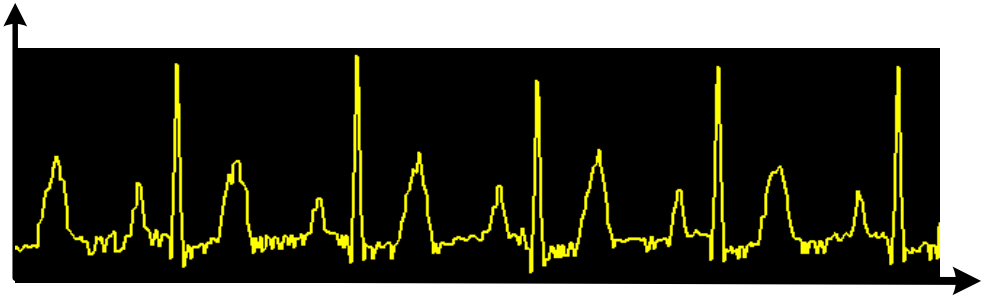
- ECG simulator

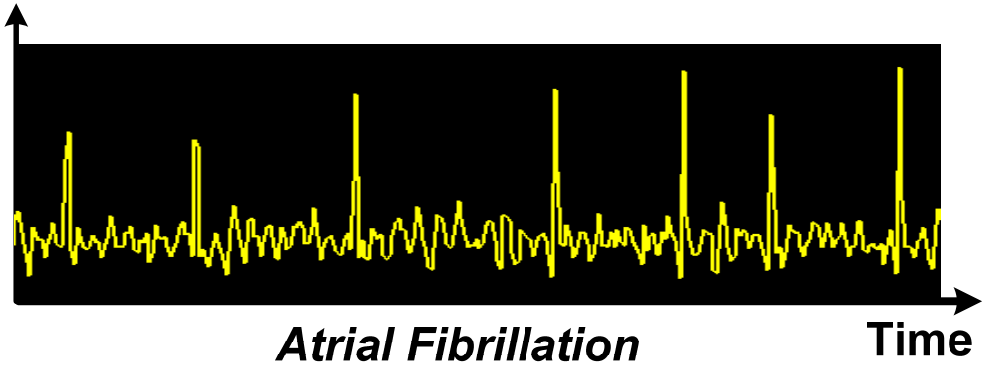


Fluke



Amplifier Output



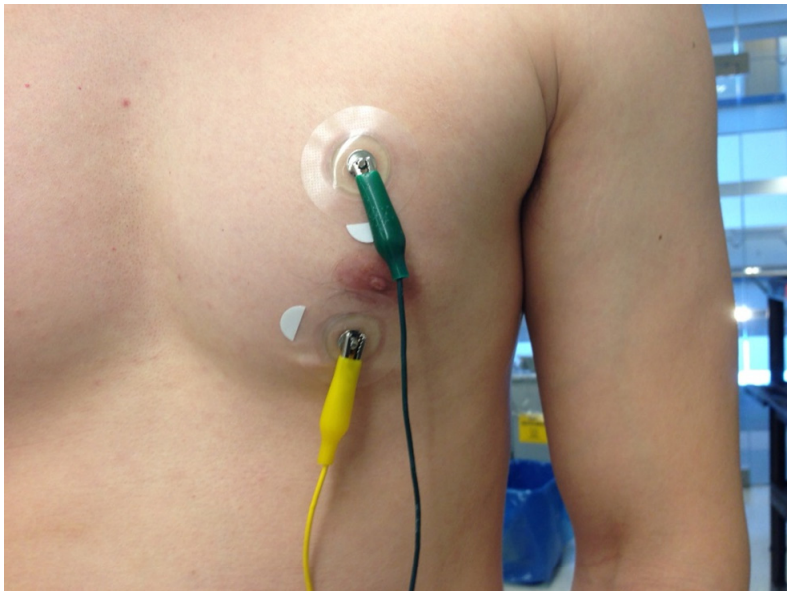


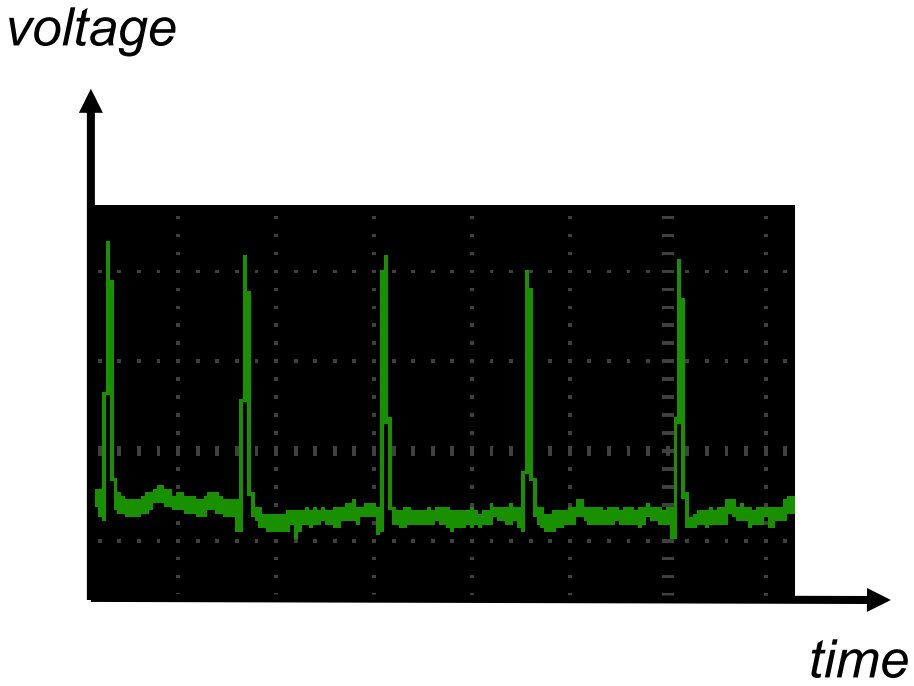
Measured Waveforms Stored in Digital Back End

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Measurement Results

- Human chest
 - 2 ECG patches 5cm apart

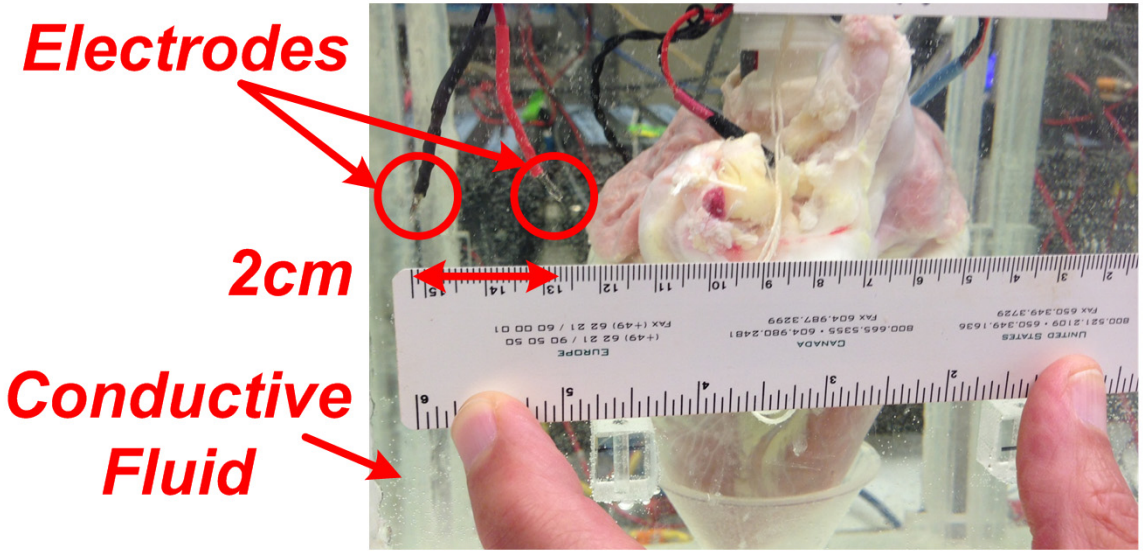


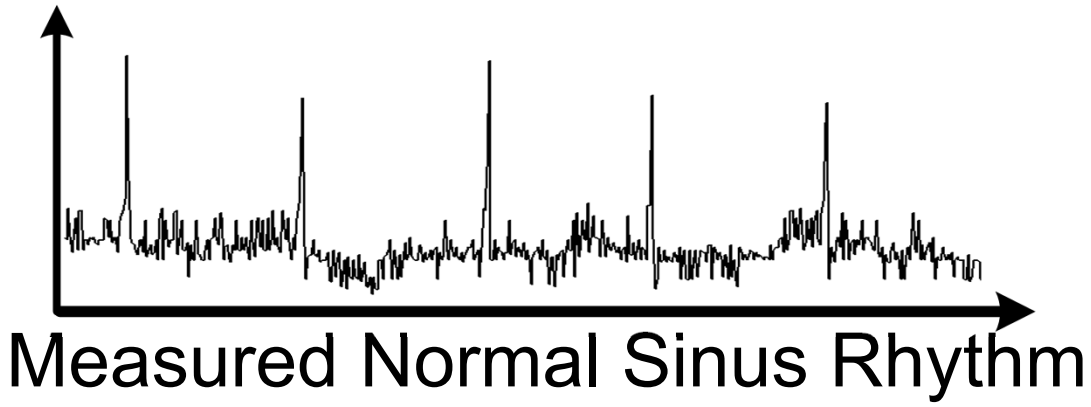


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Measurement Results

- Isolated live sheep heart





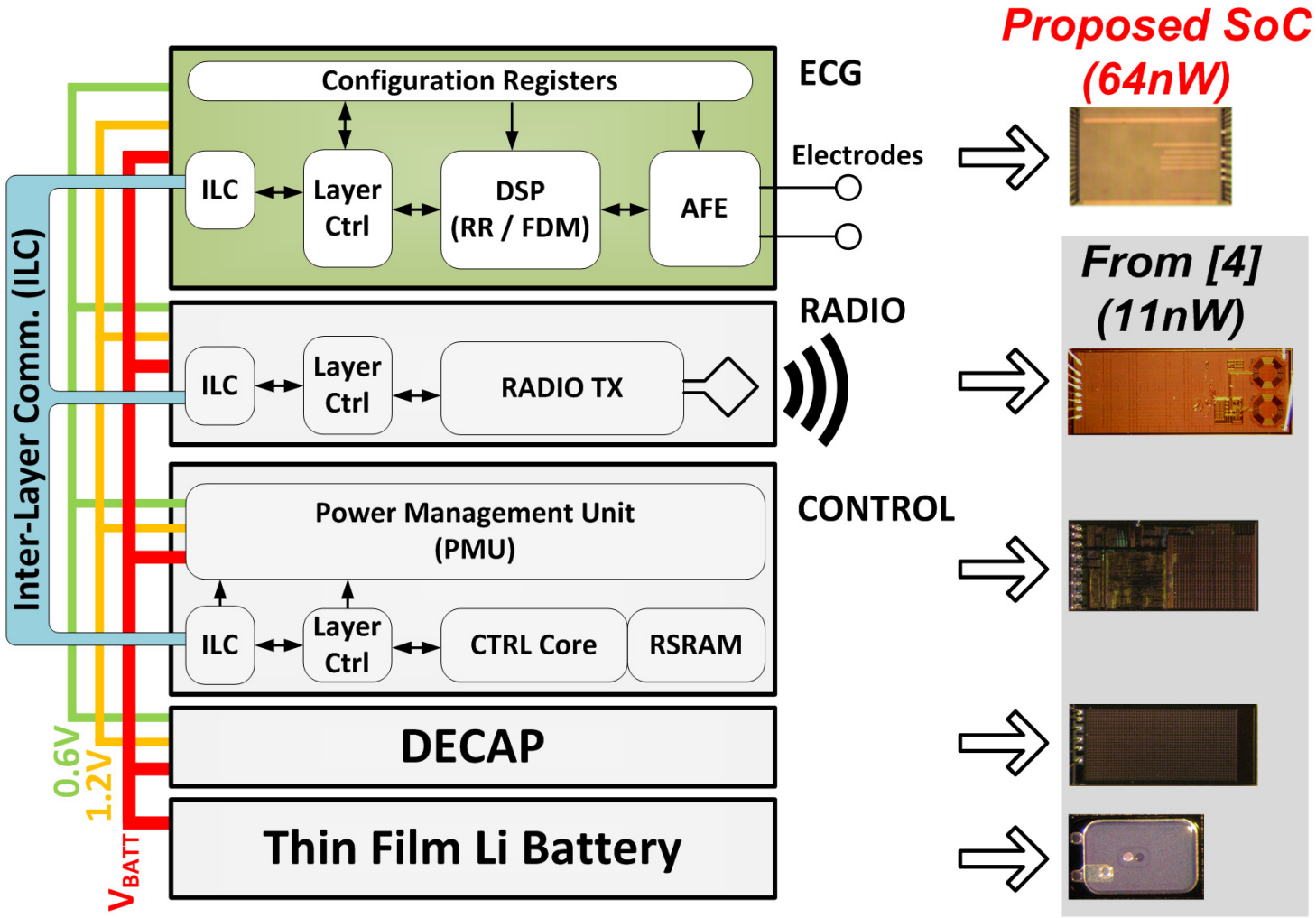
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Comparisons

		This Work	Zhang, ISSCC '12	Hsu, VLSI '12	Kim, ISSCC '13
Target Signals		**ECG**	ECG, EMG, EEG	ECG, VCG, PCG	ECG, Bio-Impedance
Technology		**65 nm**	130 nm	90 nm	180 nm
AFE	V_{DD}	**0.6 V**	1.2 V	0.5 V	1.8 V
	Current	**31 nA**	4 μA	20.44 μA (8-Bit, 2kHz Sampling)	-
	Gain	**51 ~ 96 dB**	40 ~ 78 dB	40 ~ 64 dB	40 ~ 64 dB
	Bandwidth	**250 Hz**	320 Hz	0.5 ~ 1 kHz	0.5 ~ 1 kHz
	Input Referred Noise	**253 nV/√Hz**	-	-	200 nV/√Hz
	ADC Bits	**8 Bits**	8 Bits	8/12 Bits	9.3 Bits (ENOB)
	ADC Sampling Frequency	**500 Hz**	-	250 Hz ~ 100 kHz	-
DSP	V_{DD}	**0.4 V**	0.3 ~ 1.2 V	0.5V (1.0V for SRAM)	- (Analog Signal Processing)
	Power Consumption	**45 nW**	2.1 μW	-	
	Clock Frequency	**10 kHz**	2 kHz ~ 1.7 MHz	25 MHz	
System Total Power Consumption		**64 nW**	6.9 μW	22.6 μW	11.3 μW
Power Calculation Configuration		**AFE + DSP Arrhythmia Detection (FDM)**	AFE + DSP R-R Extraction	AFE (BSI) + DSP + OSC Arrhythmia Detection	AFE (3ch ECG + RA) + ASP + OSC Arrhythmia Detection

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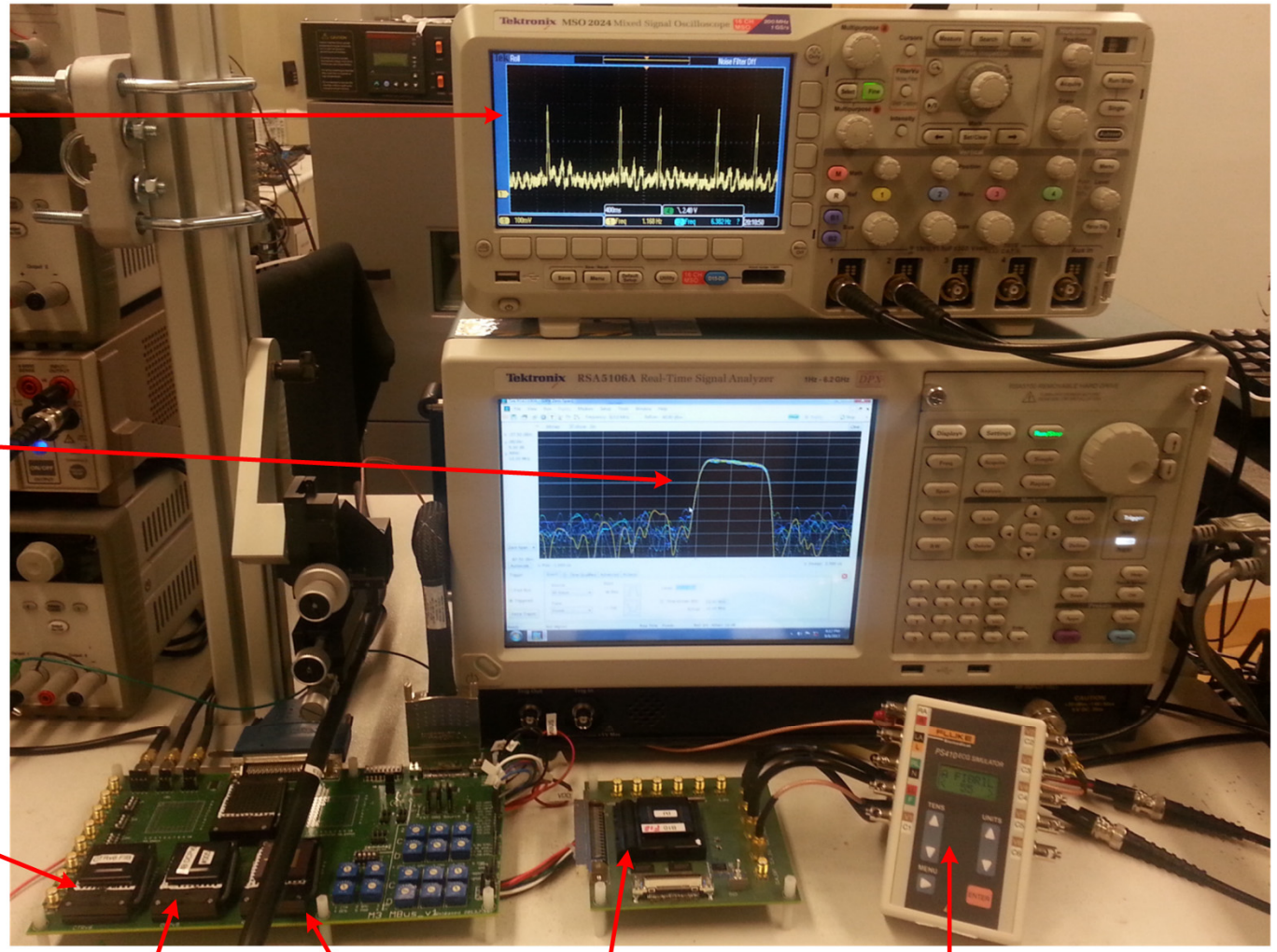
Complete System Configuration



Lee et al., ISSCC 2012

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Complete System Test



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Conclusions

- A syringe-implantable ECG monitoring systems is proposed
- Achieved lowest reported power consumption
- Noise optimization and circuit techniques enable 31nA current consumption
- Computation at V_{opt} further reduces energy by 40%

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Thank you!

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A 680nA Fully-Integrated Implantable ECG Acquisition IC with Analog Feature Extraction

Long Yan, Ph.D.

Pieter Harpe, Masato Osawa, Yasunari Harada,

Kosei Tamiya, Chris Van Hoof, Refet Firat Yazicioglu

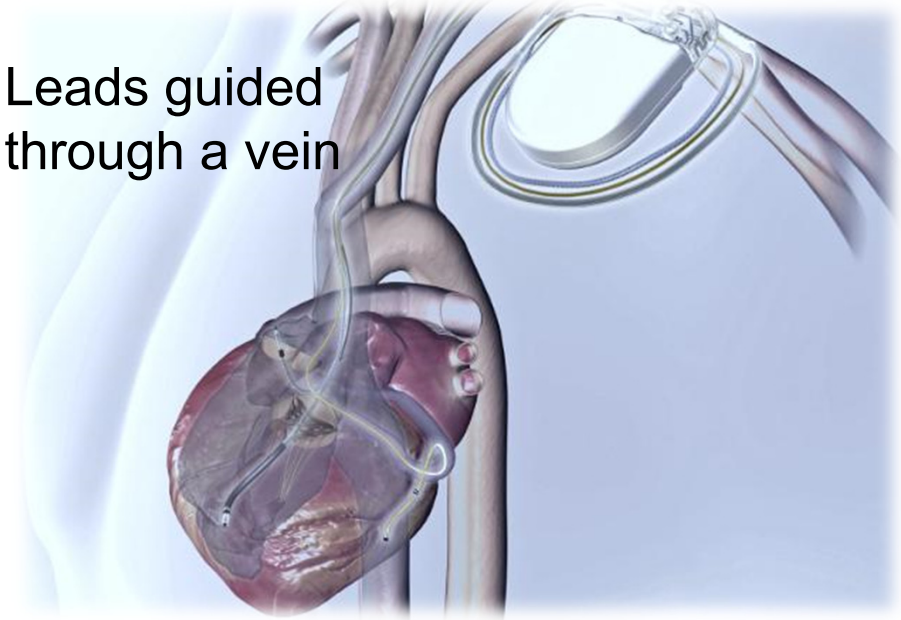






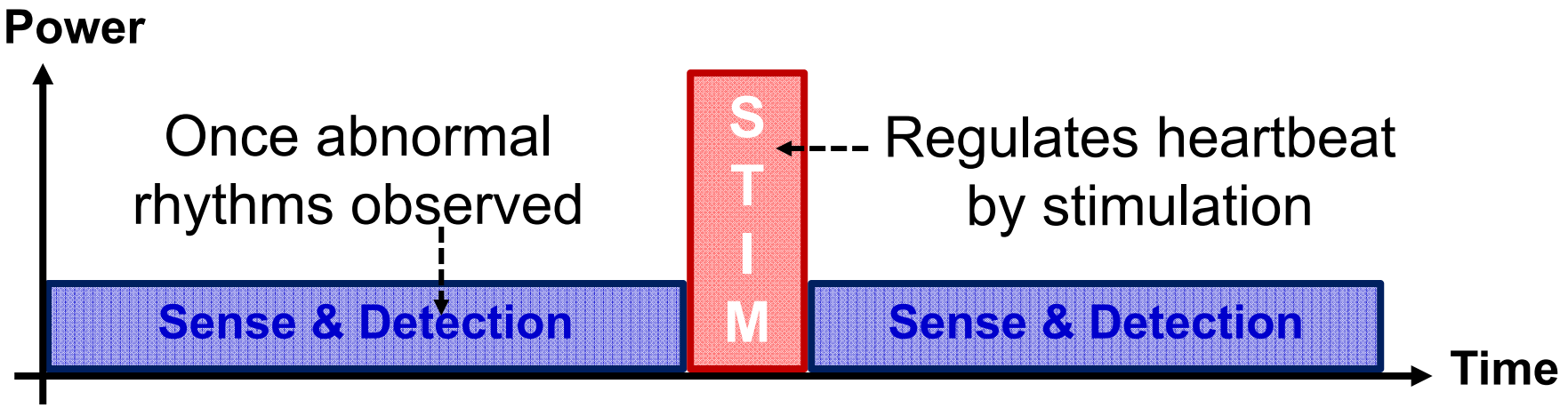
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Implantable Cardiac Pacemaker



40% of all human deaths
are attributed to
cardiovascular diseases.

More than 250,000
pacemaker implants every year

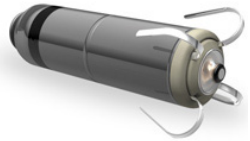


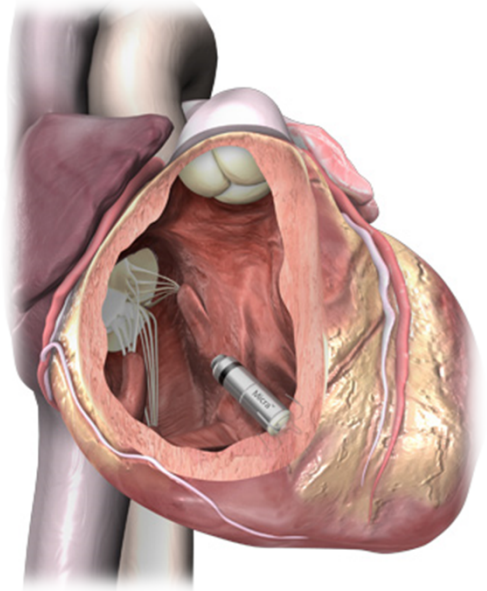
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Tiny pacemaker can be implanted WITHOUT SURGERY



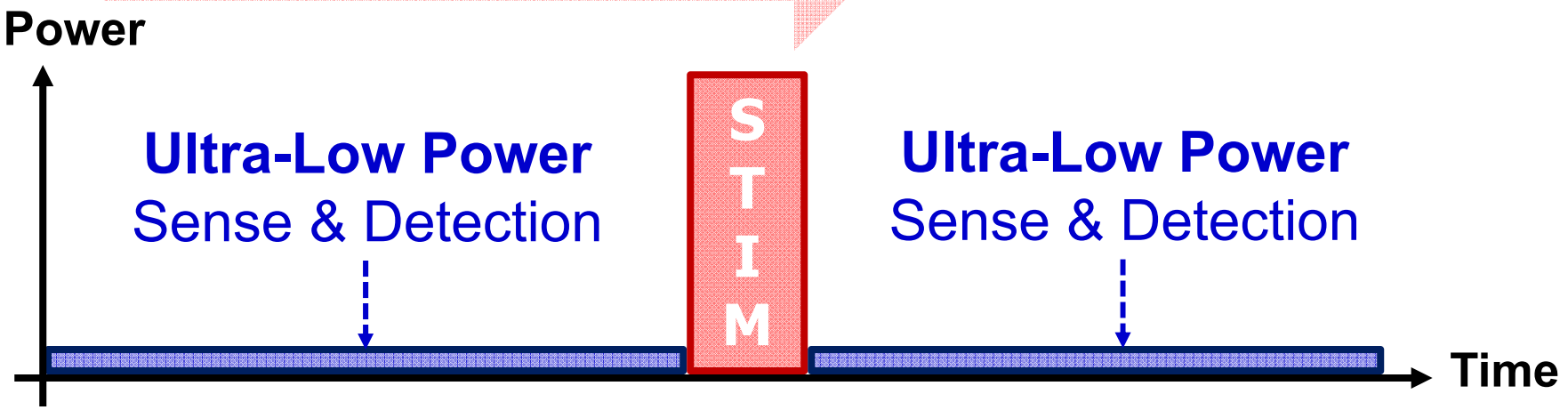
24mm Long
0.75cm^3 Volume





TODAY ULP IC + μ-Battery FUTURE

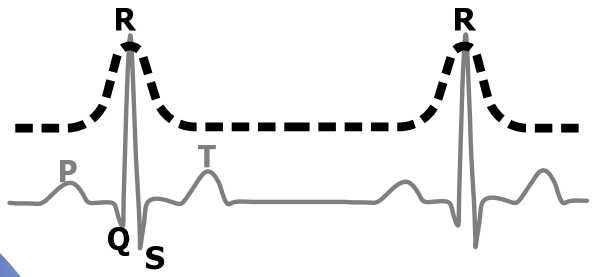
1/10 Miniaturization



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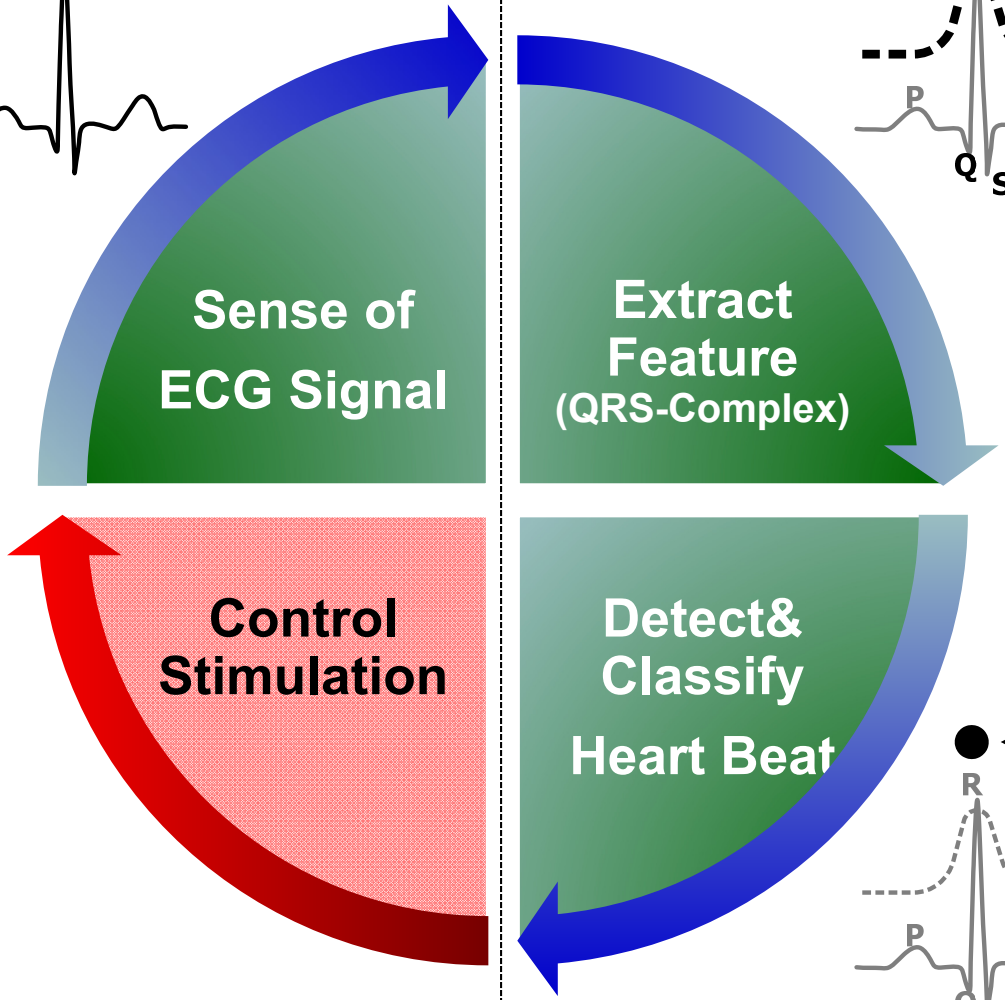
Today's Pacemaker Operation Cycle

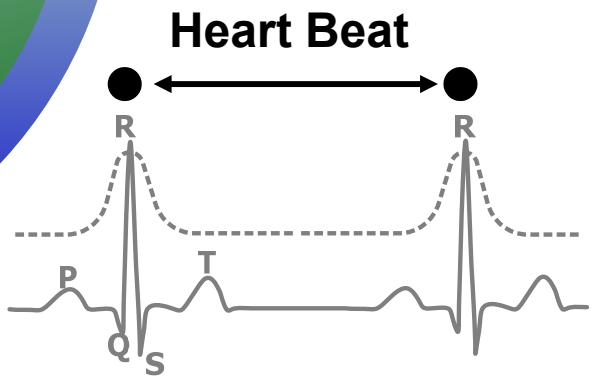




Analog
Acquisition &
Stimulation

Digital
Signal
Processing





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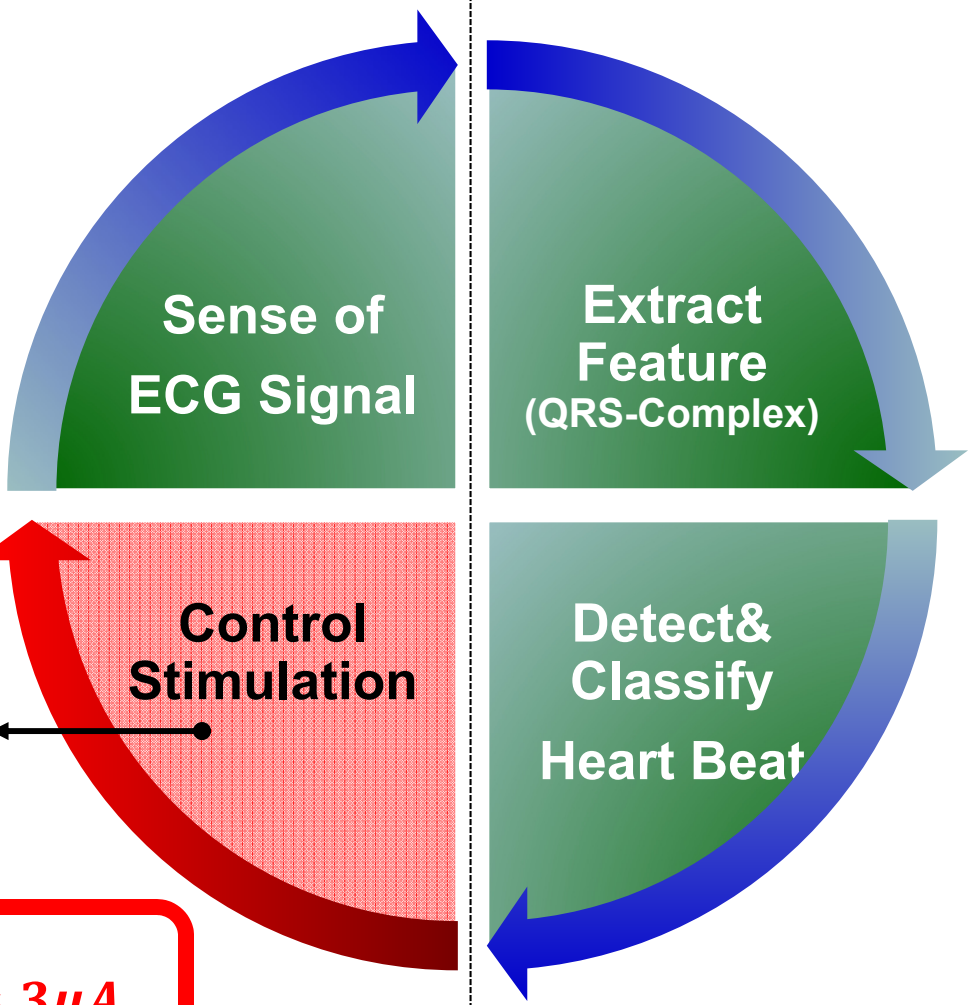
Power Budget of Pacemaker

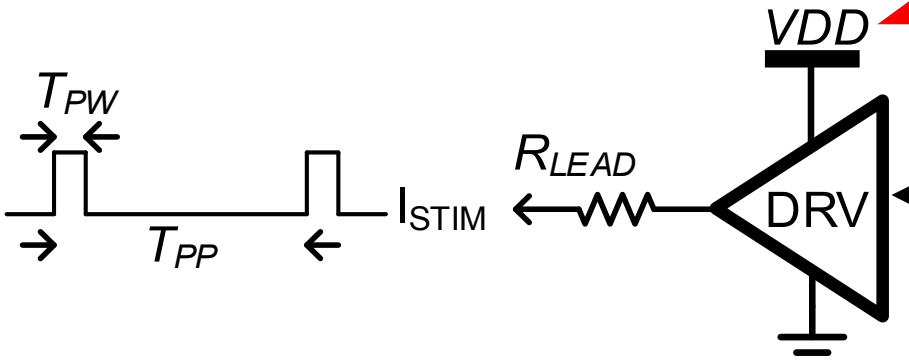
900mA-hrs ➔ 100μA-years

Lithium Battery



< 10μA
for 10 years
life span



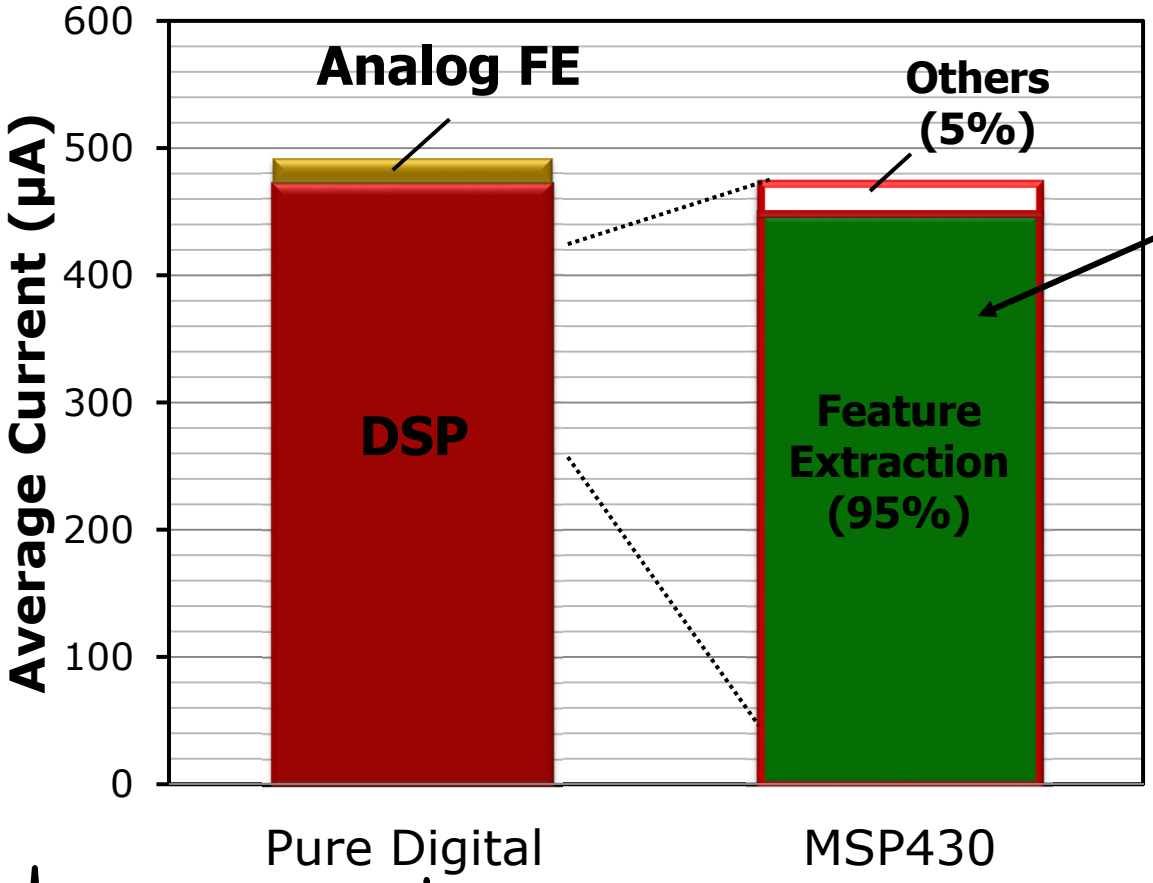


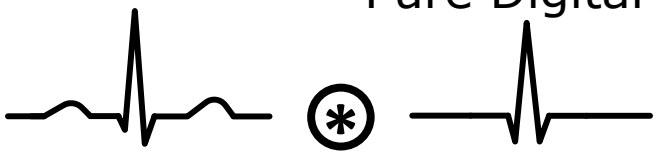
$$I_{AVG} = \frac{V_{DD}}{R_{LEAD}} \cdot \frac{T_{PW}}{T_{PP}} = \frac{2.5V}{500\Omega} \cdot \frac{0.5ms}{0.857s} \approx 3\mu A$$

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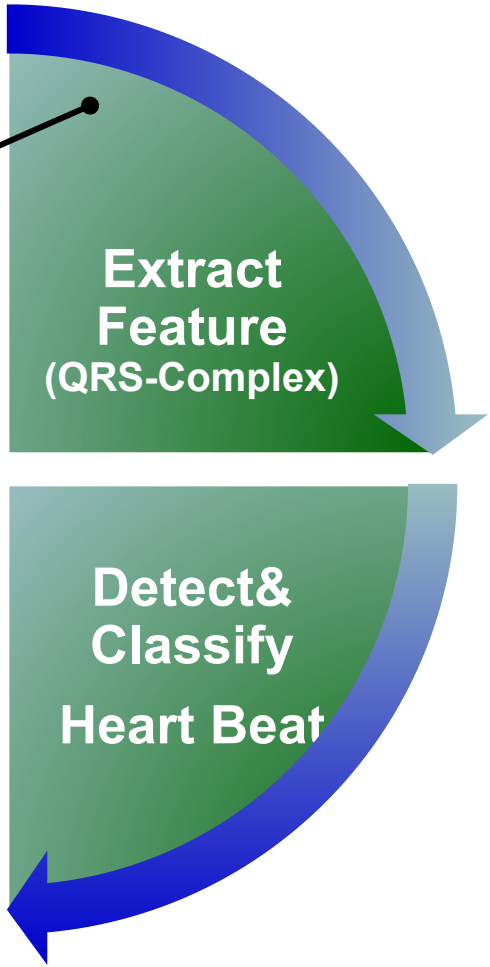
Excessive Power Consumption in DSP

[3] R.F. Yazicioglu, *ISSCC* 2010





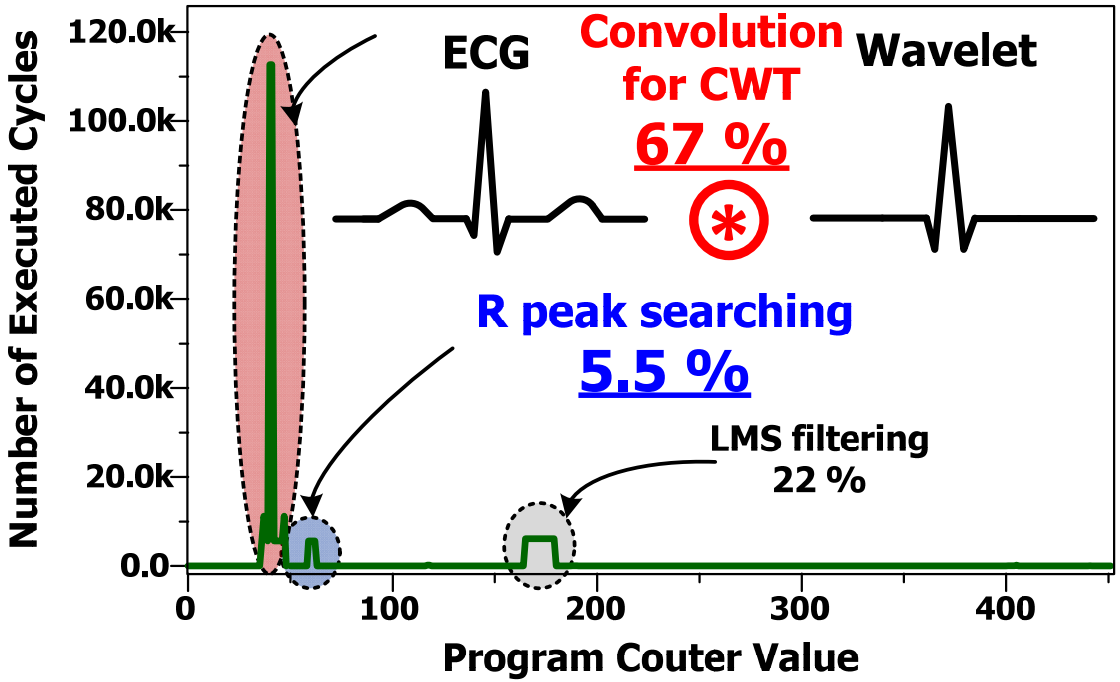
Feature Extraction based on Continuous Wavelet Transform (CWT)

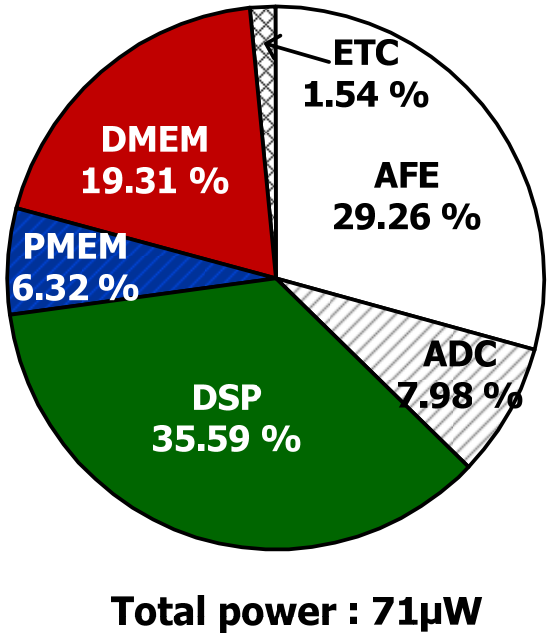


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Digital-Domain Feature Extraction

Continuous Wavelet Transform (CWT)





Total power : 71μW

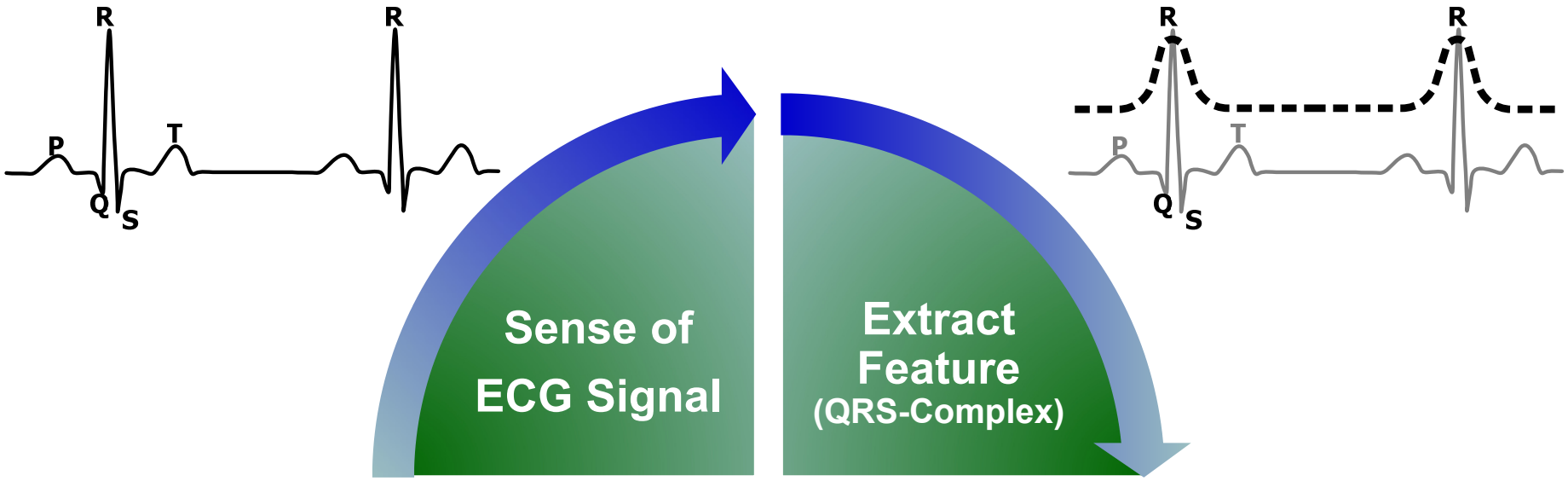
H. Kim, "A configurable and Low-Power Mixed Signal SoC...," *IEEE Trans. on BioCAS,* 2014.

High Performance but rather Power Hungry

due to its intensive Multiply-Accumulate (MAC) operation

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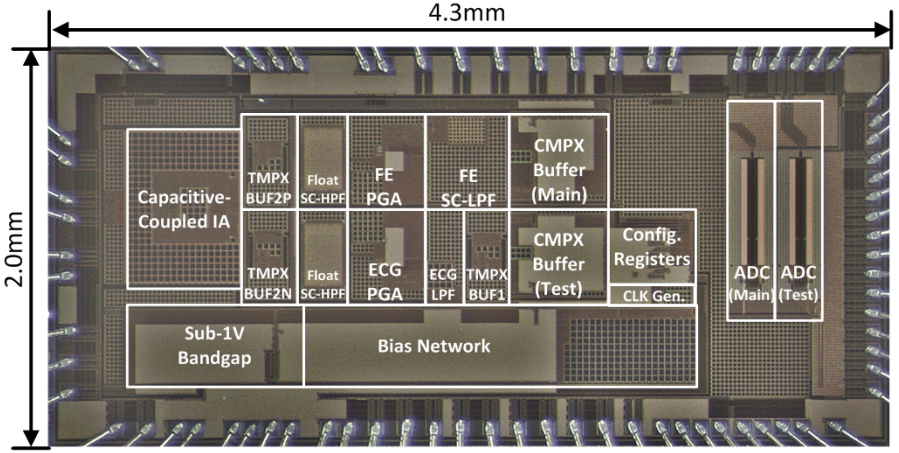
This Work



Analog

Feature Extraction

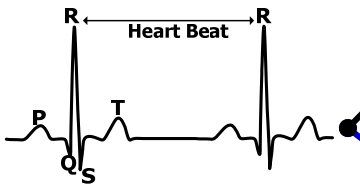
Acquisition **< 1µA**

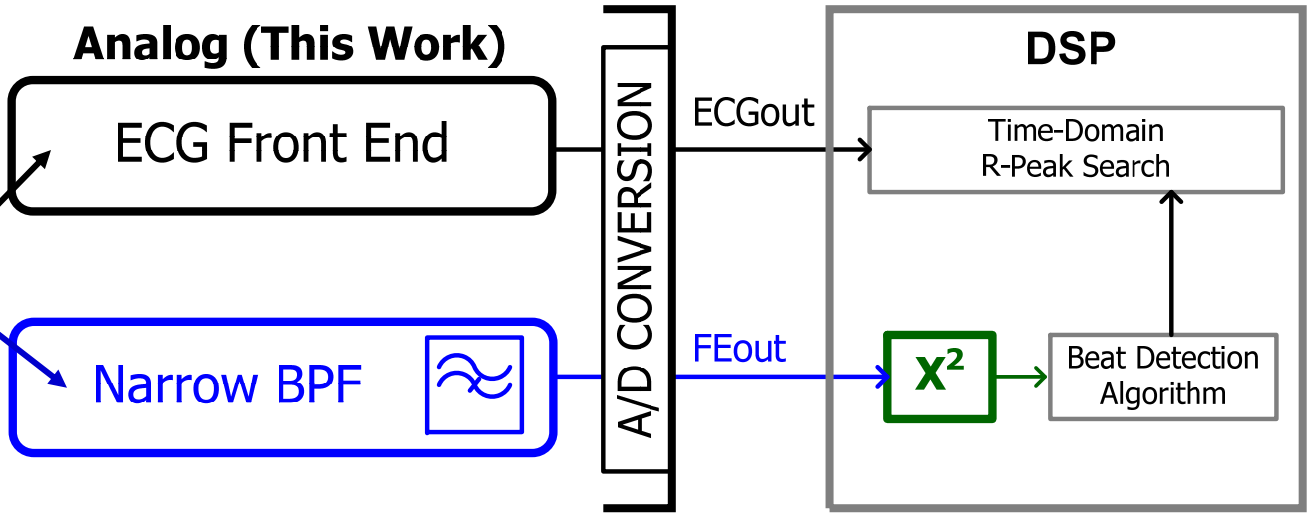


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Power Efficient Analog-Domain Feature Extraction (FE)

[8] Ann Arbor Electrogram Libraries, [Online] http://www.electrogram/com

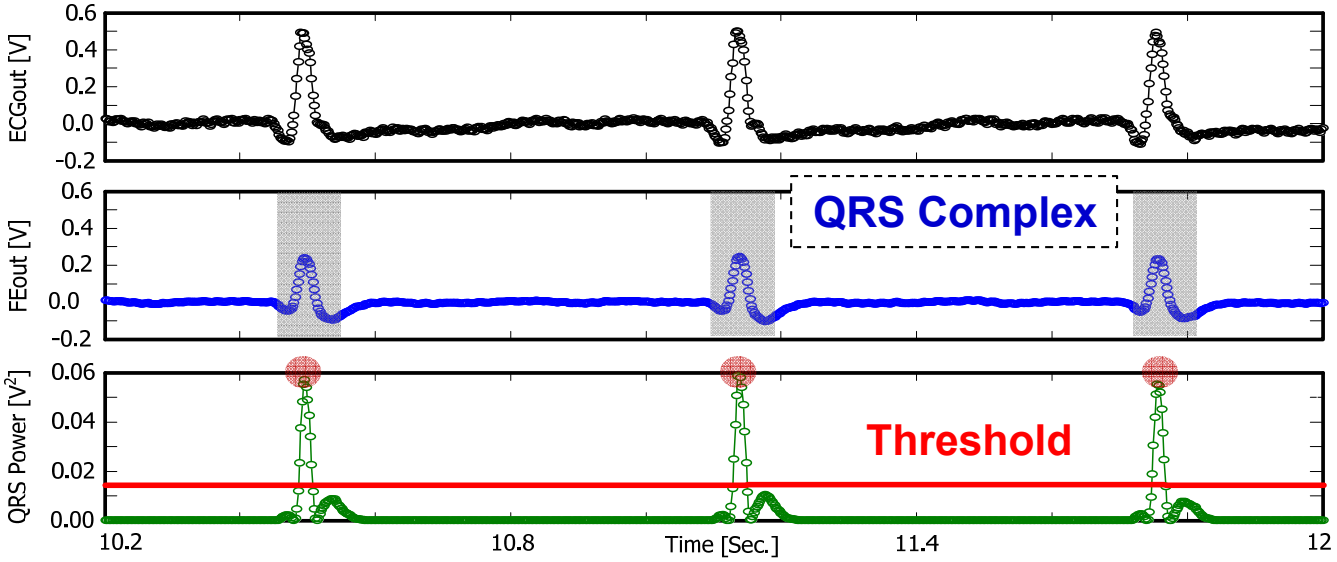




Time-domain ECG

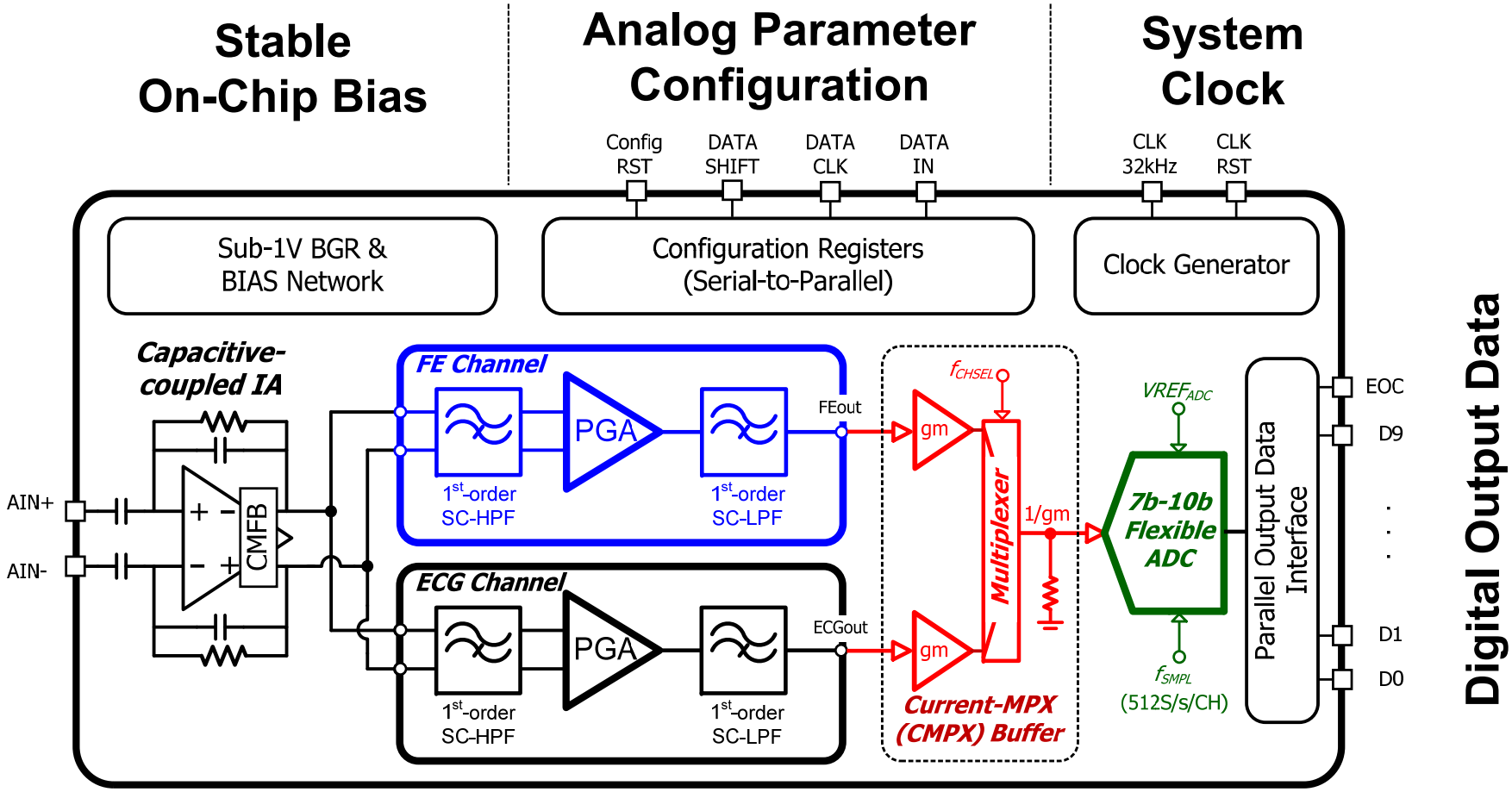
Analog FE

(FE)² & Threshold



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ASIC Architecture & Feature



- Power-Noise Efficient
- Rail-to-Rail
- On-chip

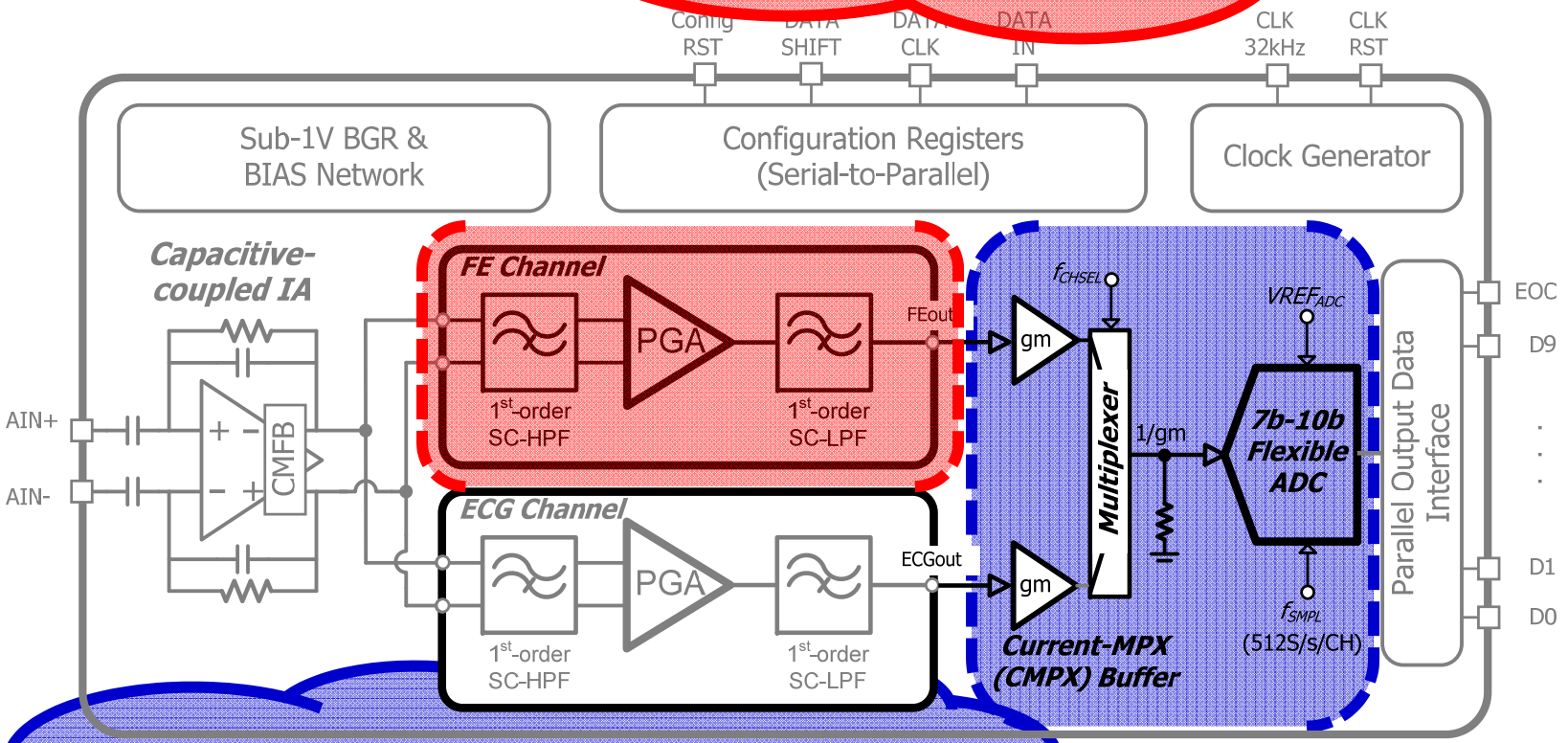
- Analog Feature Extraction
- Diff.-to-Single

- Low-Power Channel Multiplexing & Data Conversion

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Challenges:

- Features @ 1Hz-25Hz
 - ➔ **Precise & Flexible frequency selection**
 - ➔ **Low-power, small area**



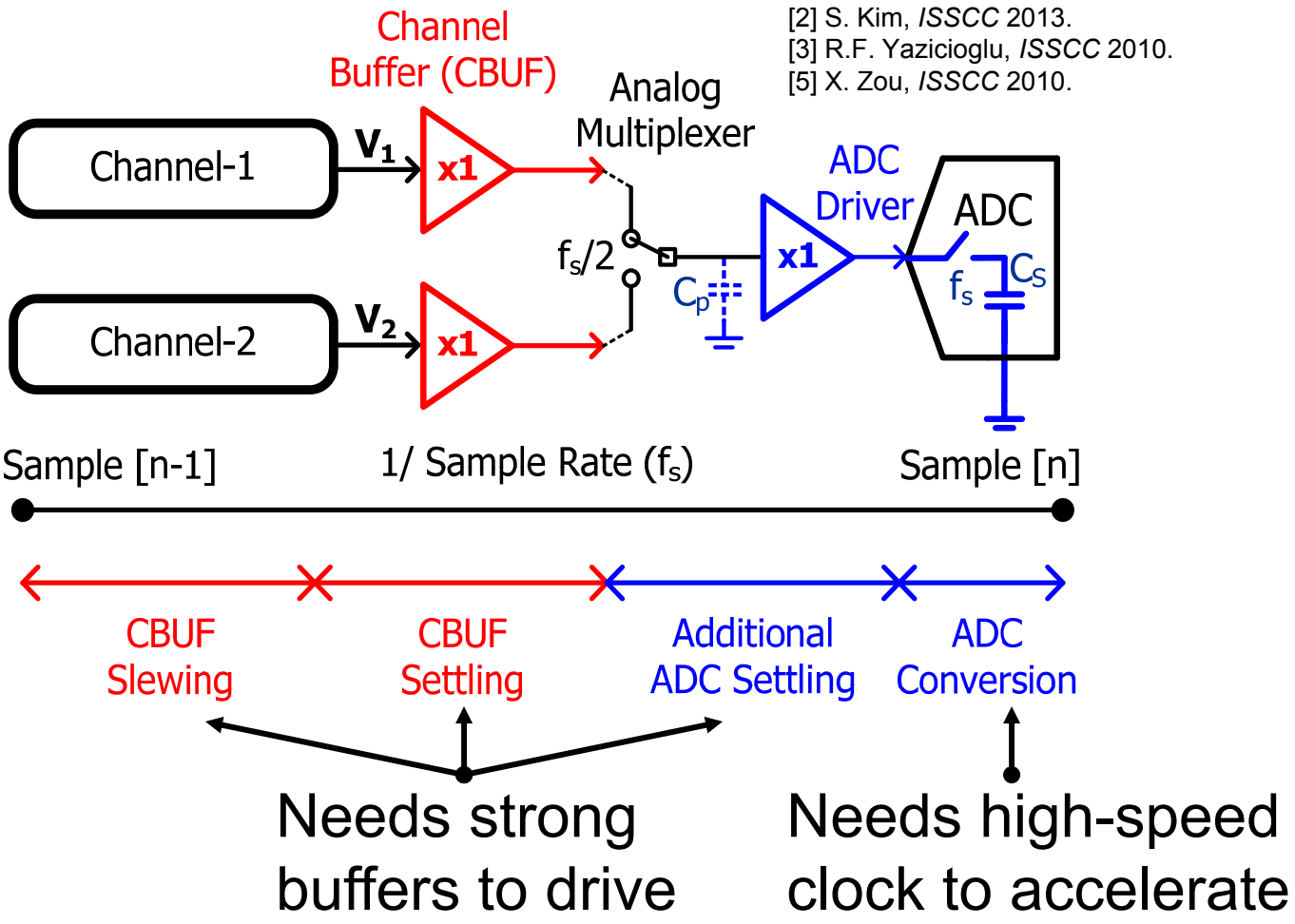
- Time-multiplexed data acquisition
 - ➔ **More analog buffers to meet speed constraints.**

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Issues on Channel-Multiplexing

Design is driven by speed considerations

to settle analog signal with enough precision < 1LSB of ADC

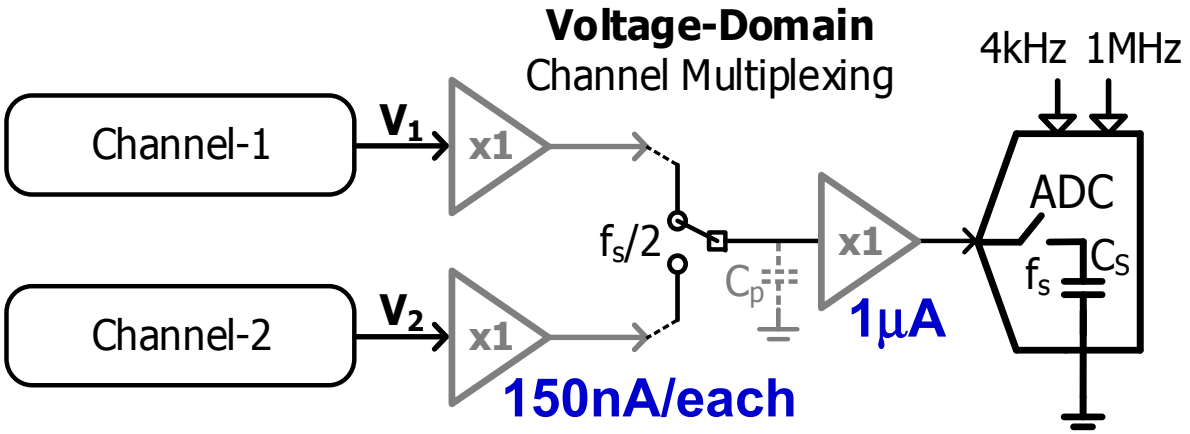


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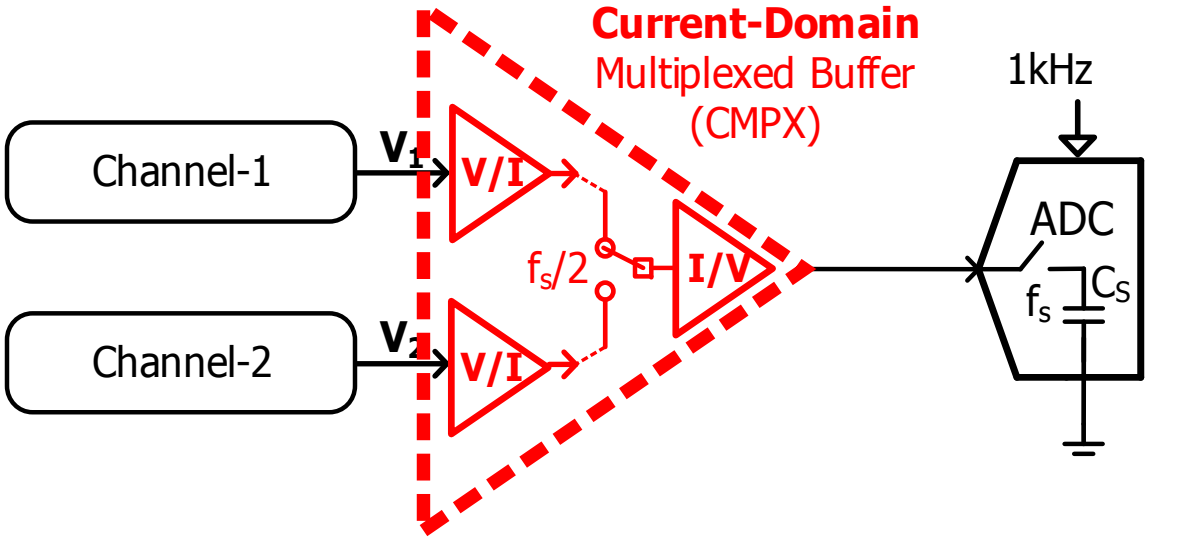
Low-Power Channel Multiplexing

[2] S. Kim, *ISSCC* 2013.

Lost more than
1year
device life span



This Work

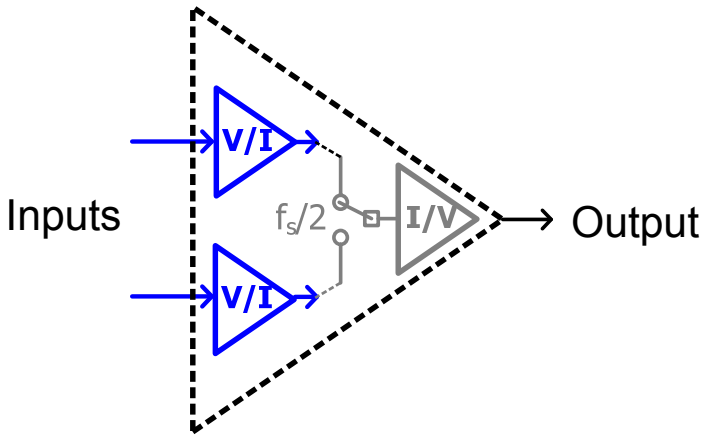


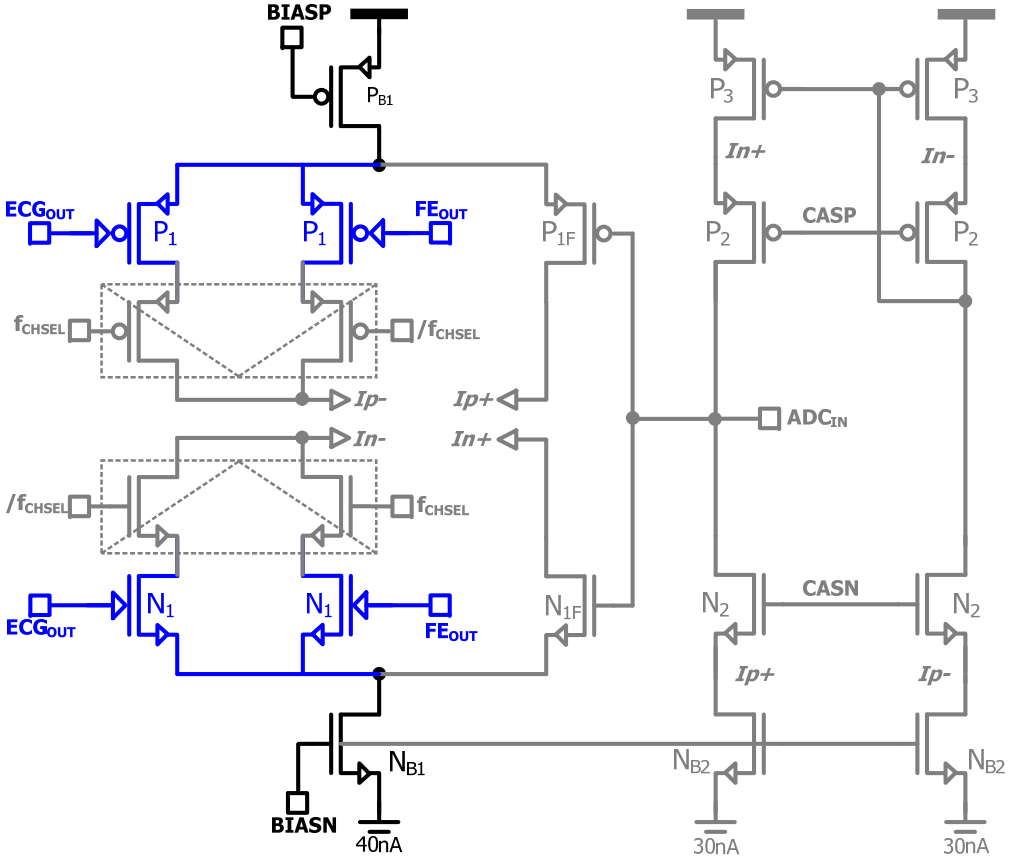
Switching channel outputs @ current-domain

➔ **Saves power of 2 channel buffers**

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Current-Multiplexed (CMPX) ADC Driver

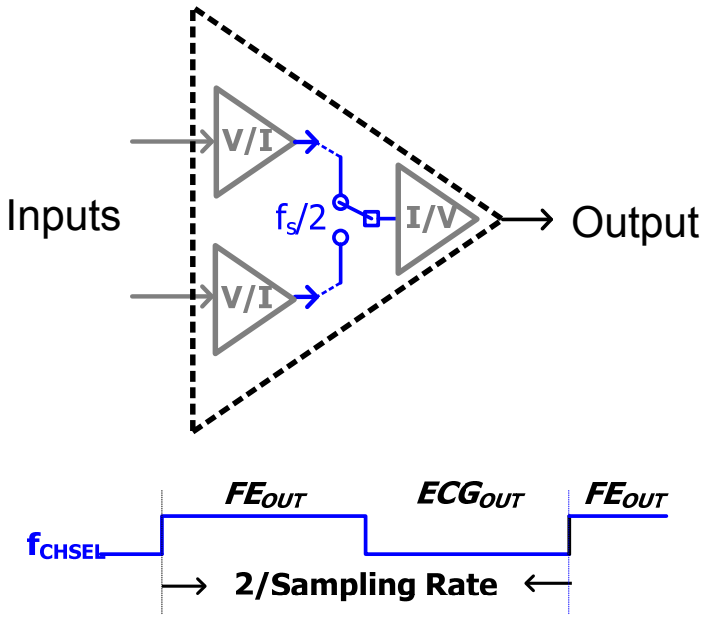


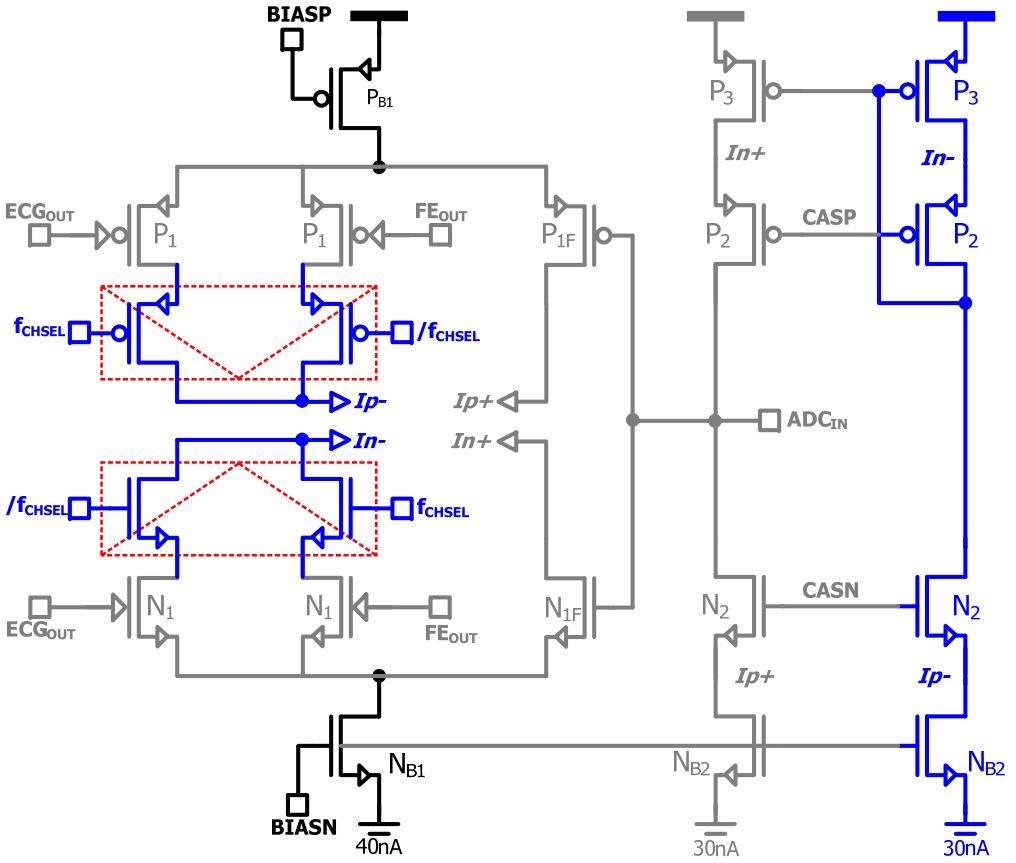


- Voltage-to-Current Conversion ➔ High Z_{in}
- Complementary Input Stage ➔ Large V_{in}

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Current-Multiplexed (CMPX) ADC Driver

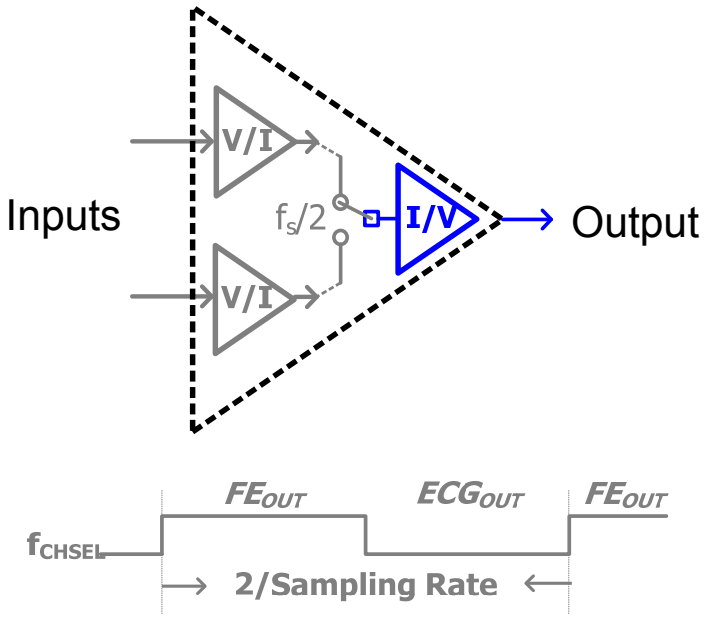


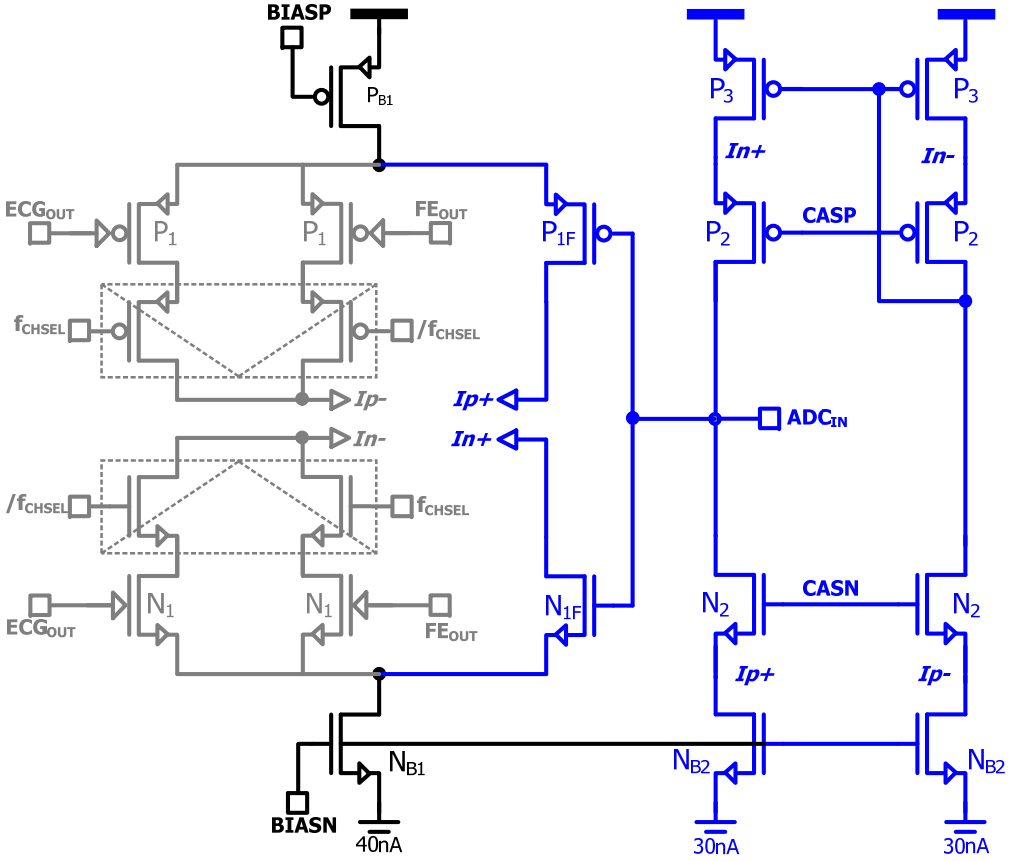


- Power Efficient Switching @ Current-Domain
- P2 & N2 act as Current Buffers

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Current-Multiplexed (CMPX) ADC Driver



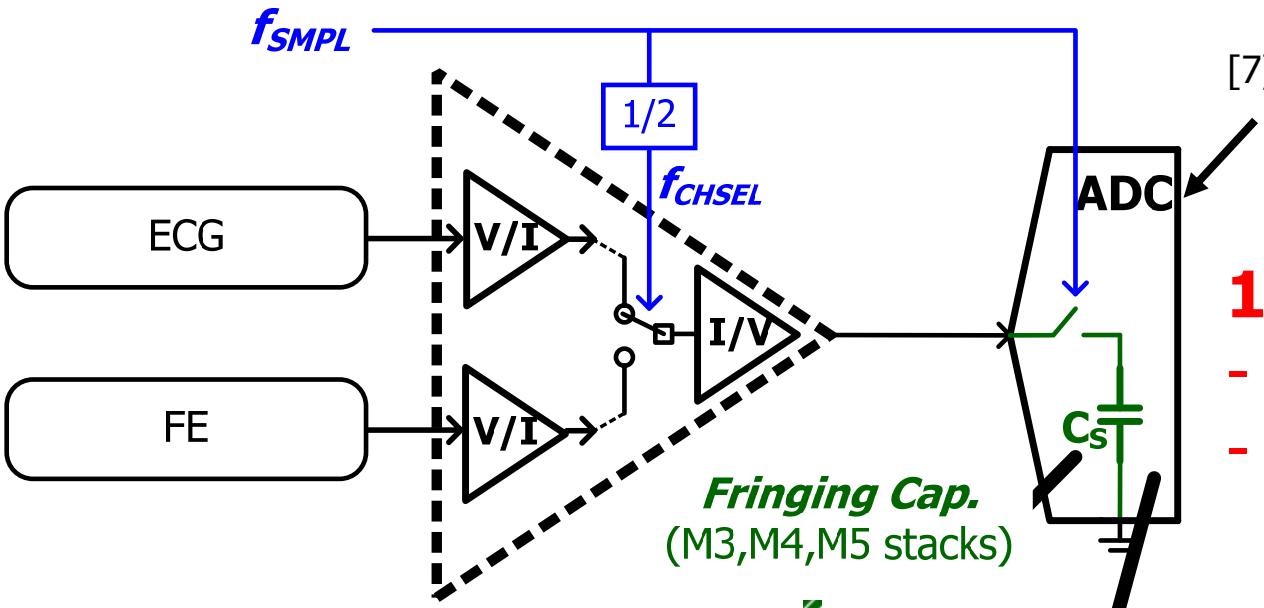


- Folded-Cascode Output Stage
 - ➔ Current-to-Voltage Conversion

$$\textbf{Gain} = Gm_1 \times (1/Gm_{1F})$$

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Power-Efficient DATA Conversion

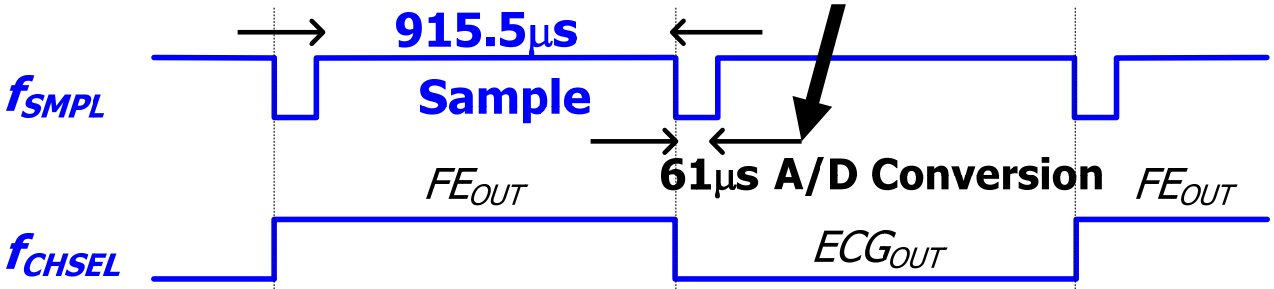


[7] P. Harpe "A 7to-10bit 0-to-4MS/s Flexible SAR ADC..., " ISSCC, pp. 472-473, 2012.

12nA @ 1kS/s,10b
- Asynchronous
- Custom CDAC

CMPX Buffer: 100nA
BW> 10kHz
@ Cs=2pF

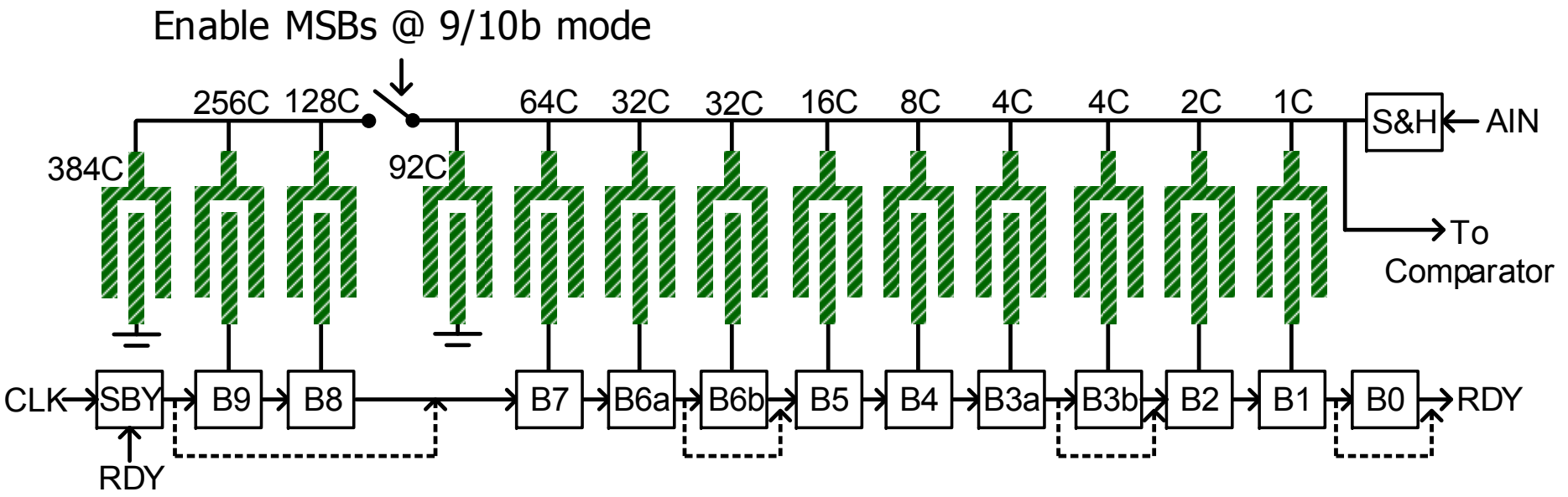
More than enough for
Asynchronous SAR Logic



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Low-Power 7-10b SAR ADC

[7] P. Harpe "A 7to-10bit 0-to-4MS/s Flexible SAR ADC..., " ISSCC, pp. 472-473, 2012.

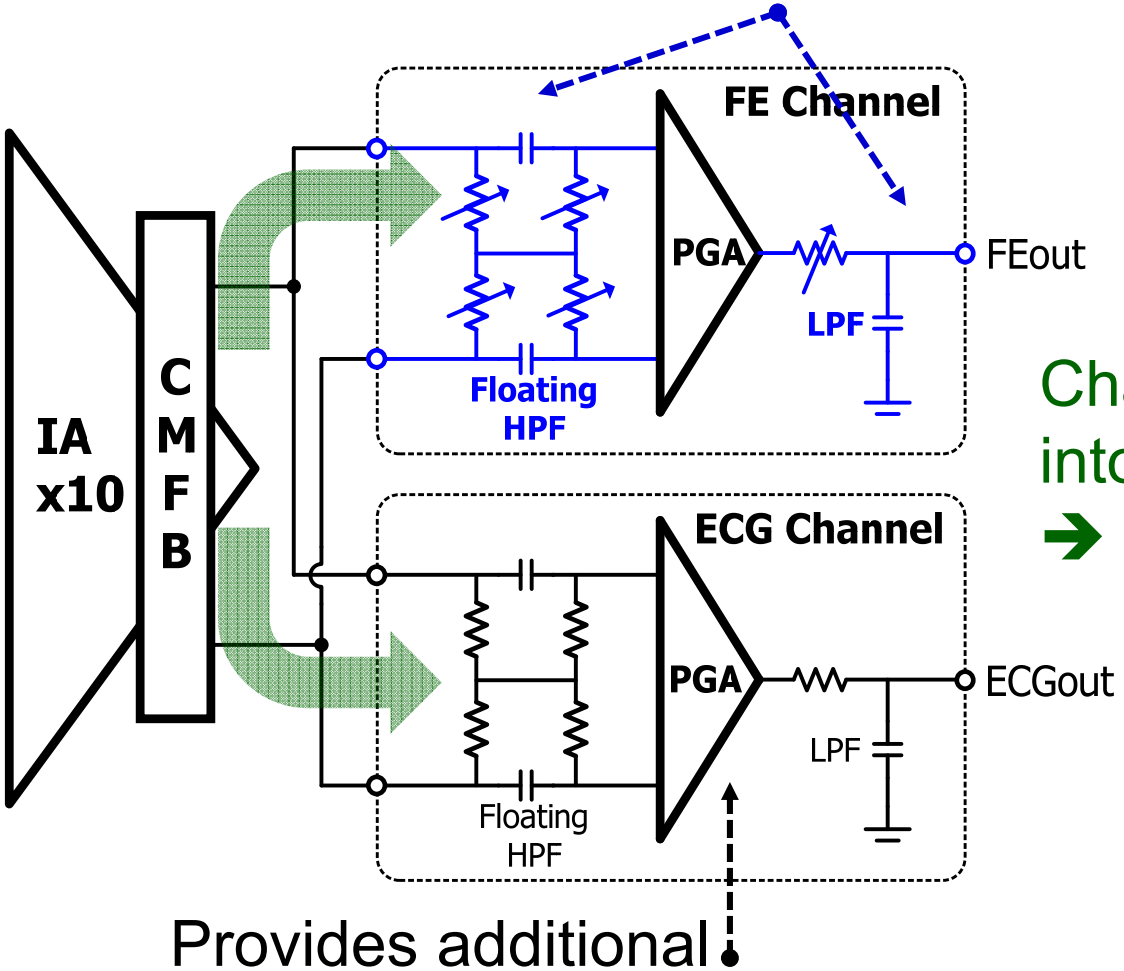


- 9bit CAP array acts as C_S & CDAC in 10b SAR ADC
 - 2modes : 9/10bit or 7/8bit
 - Custom C_{unit}=2fF ➔ C_{SMPL}=2pF @ 9/10bit mode ($SNR_{KT/C}$>70dB)
 - 12 nA @ 1kS/s,10b mode (Asynchronous, Dynamic)

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ECG & Feature Extraction Readout

FE Channel provides more
Flexibilities in BW selection

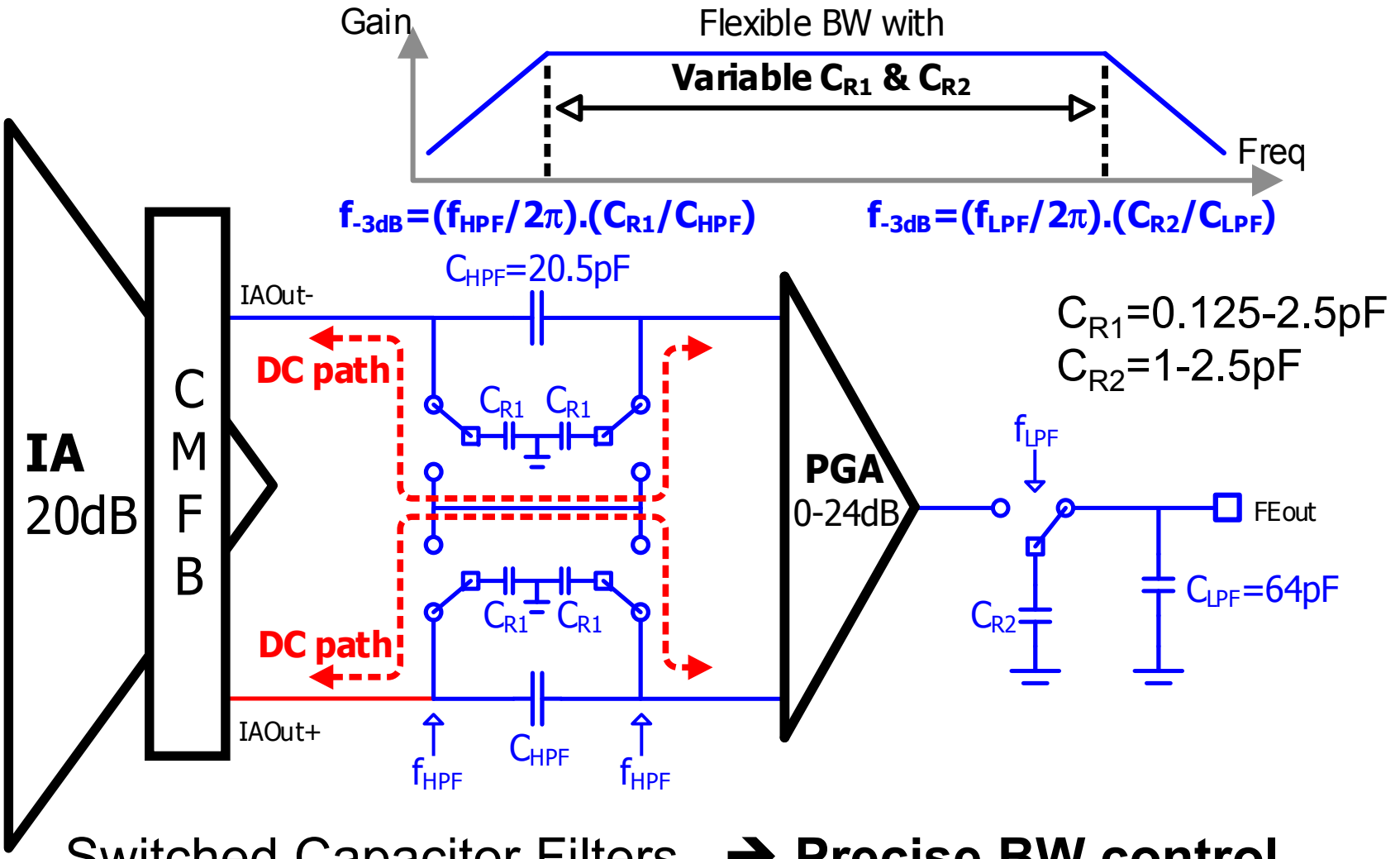


Channels branch into 2 after IA
➔ **ECG & Analog FE**

Provides additional
Programmable Gain

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Variable BW in FE Channel

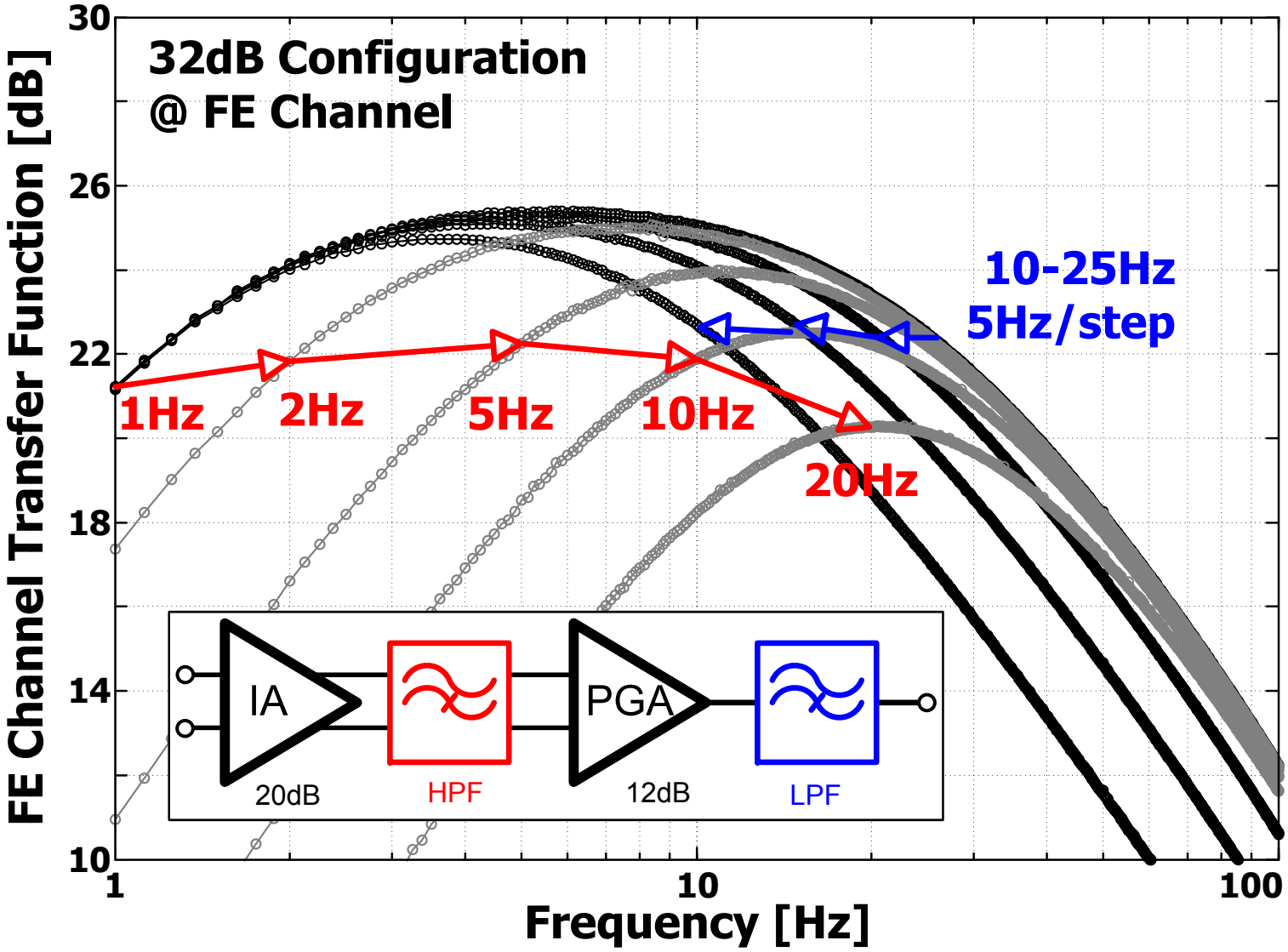


Switched Capacitor Filters ➔ **Precise BW control**

Floating HPF bypasses DC ➔ **No additional DC bias**

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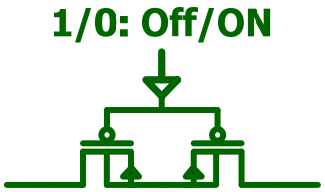
Variable BW in FE Channel



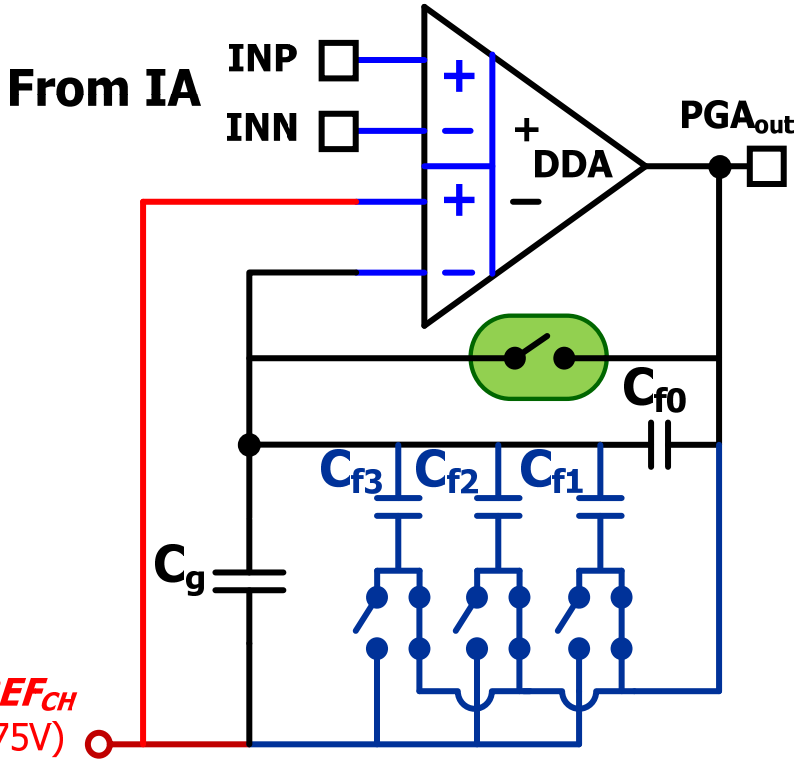
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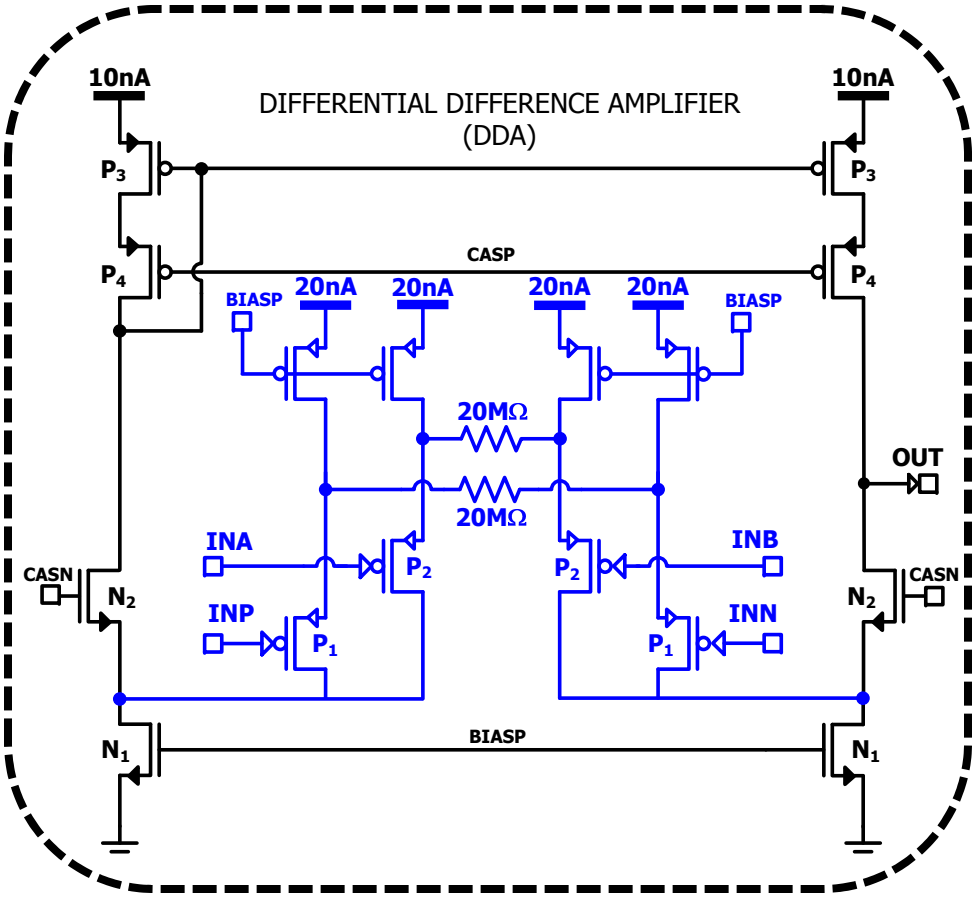
Programmable Gain Amplifier (PGA)

High R_{off}
not to deteriorate
low frequency cutoff



- 2 Identical Inputs
- Consumes only 100nA



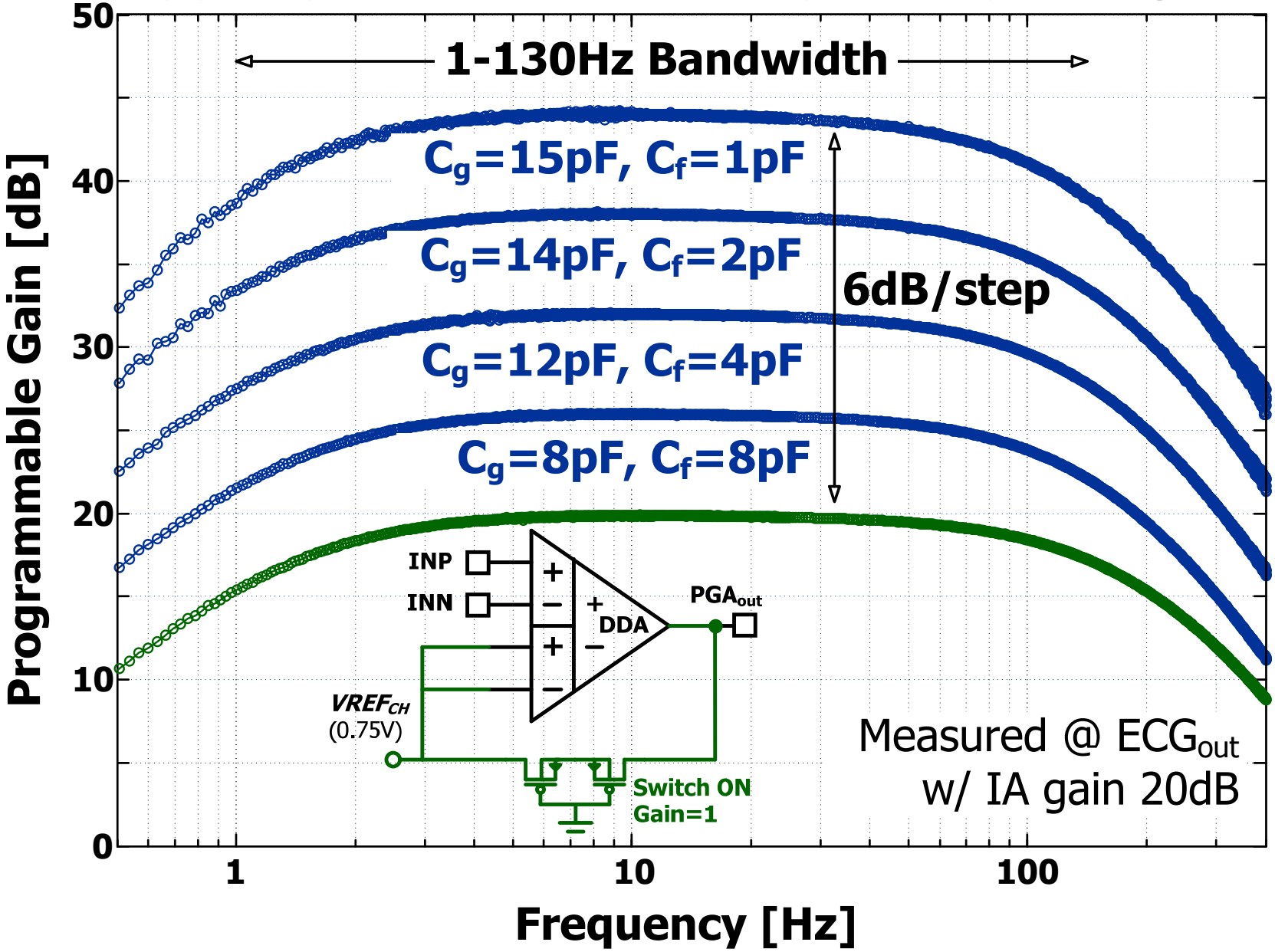


Sets Output DC Common-Mode

Flipped C_f : Gain = 1+ (C_g/C_f)

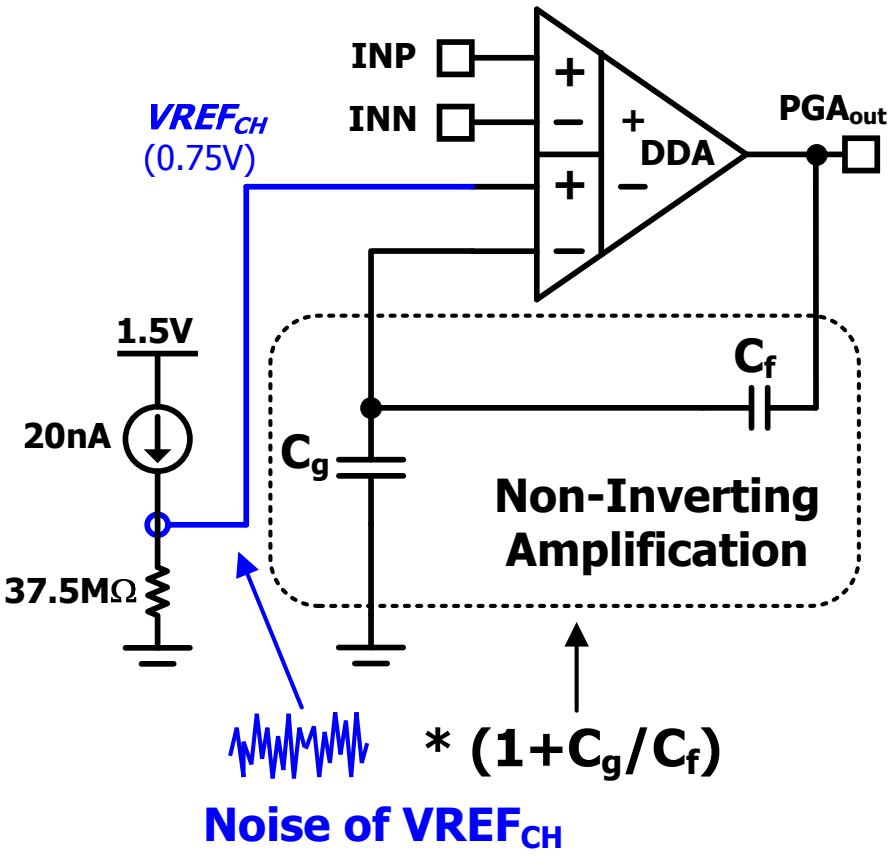
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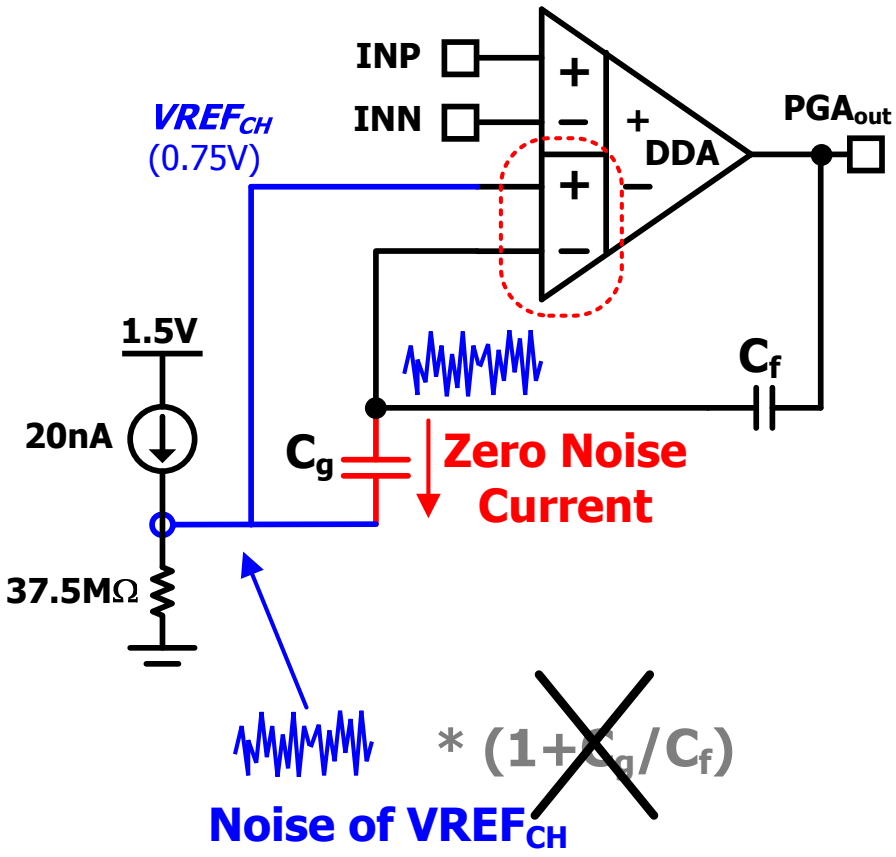
Measured Channel Transfer Function



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Noise Concerns on DC Bias



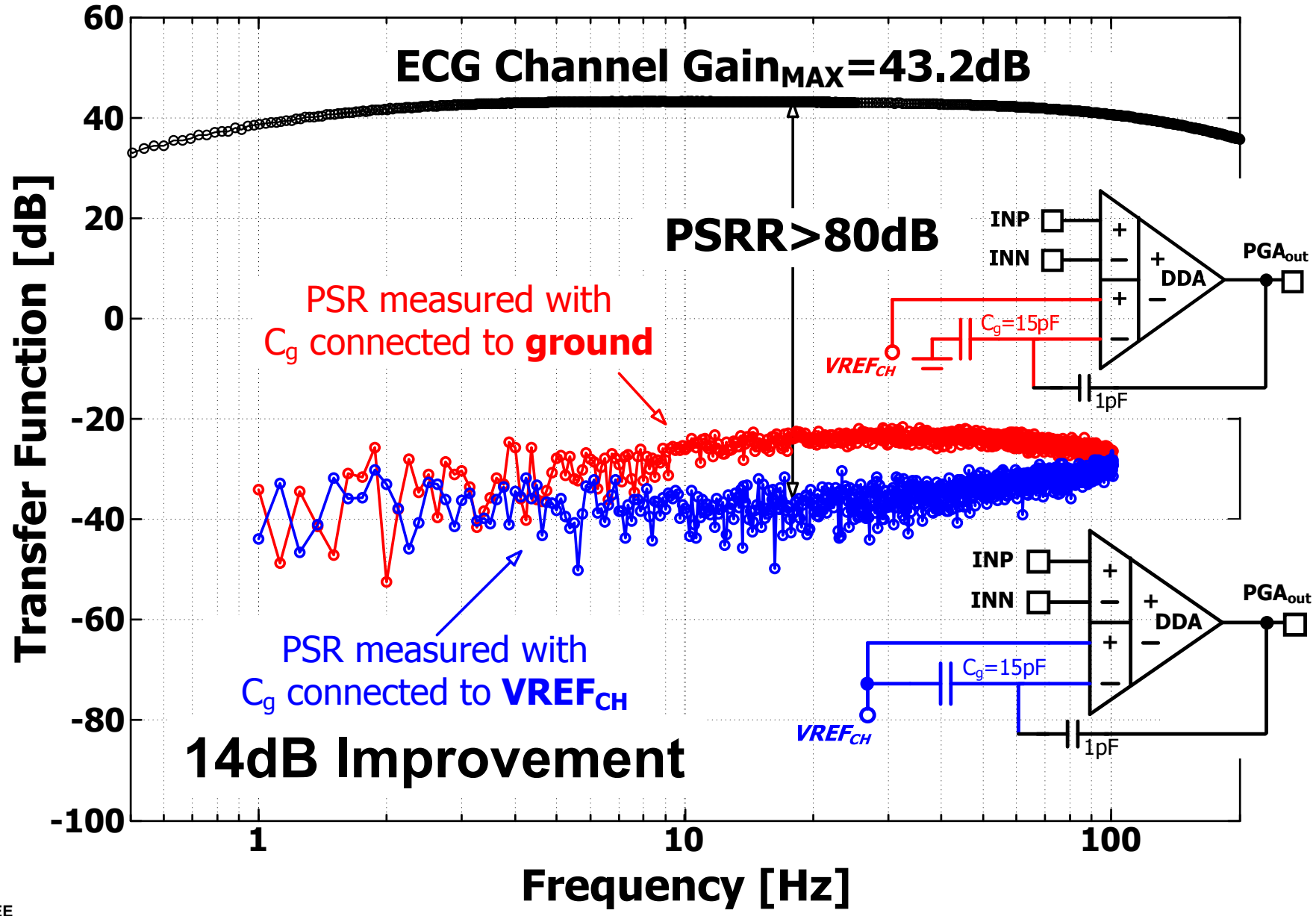


C_g is driven by the same DC bias to

avoid high-gain noise amplification

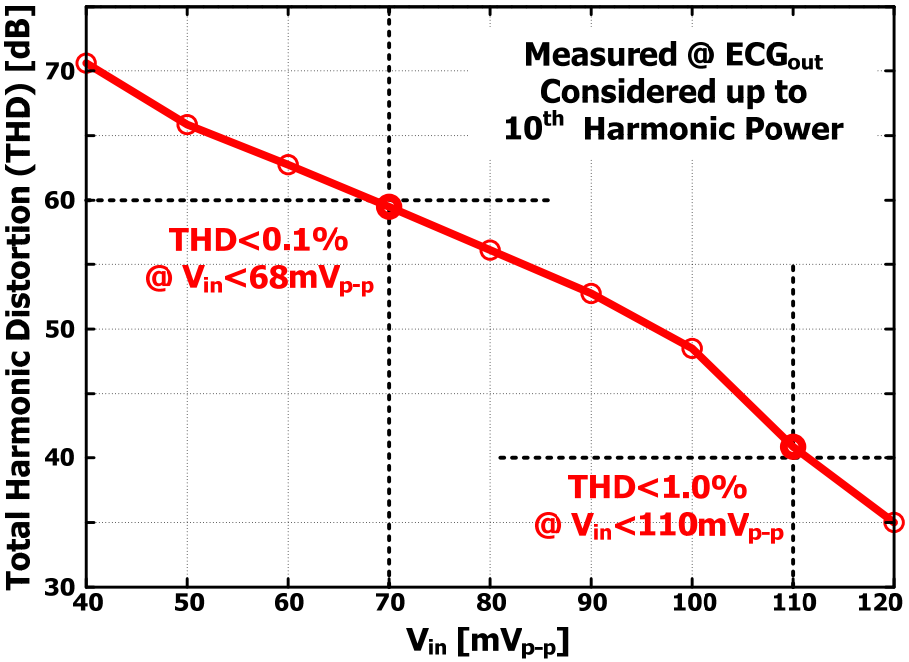
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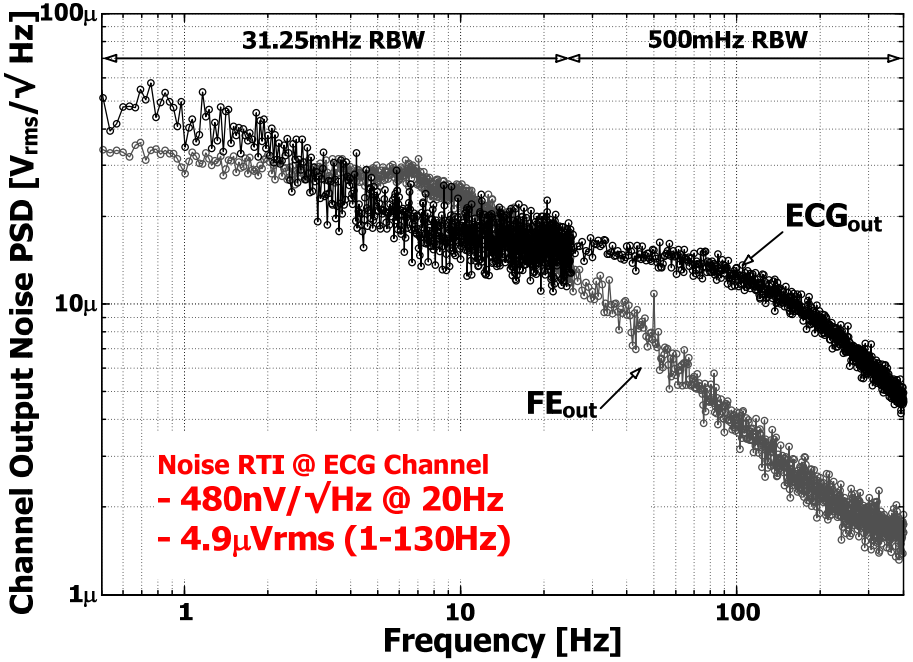
Power Supply Rejection Ratio > 80dB



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Channel Dynamic Range





Max. Input Range

68mV$_{p-p}$ @ THD=0.1%

110mV$_{p-p}$ @ THD=1.0%

Input Referred Noise

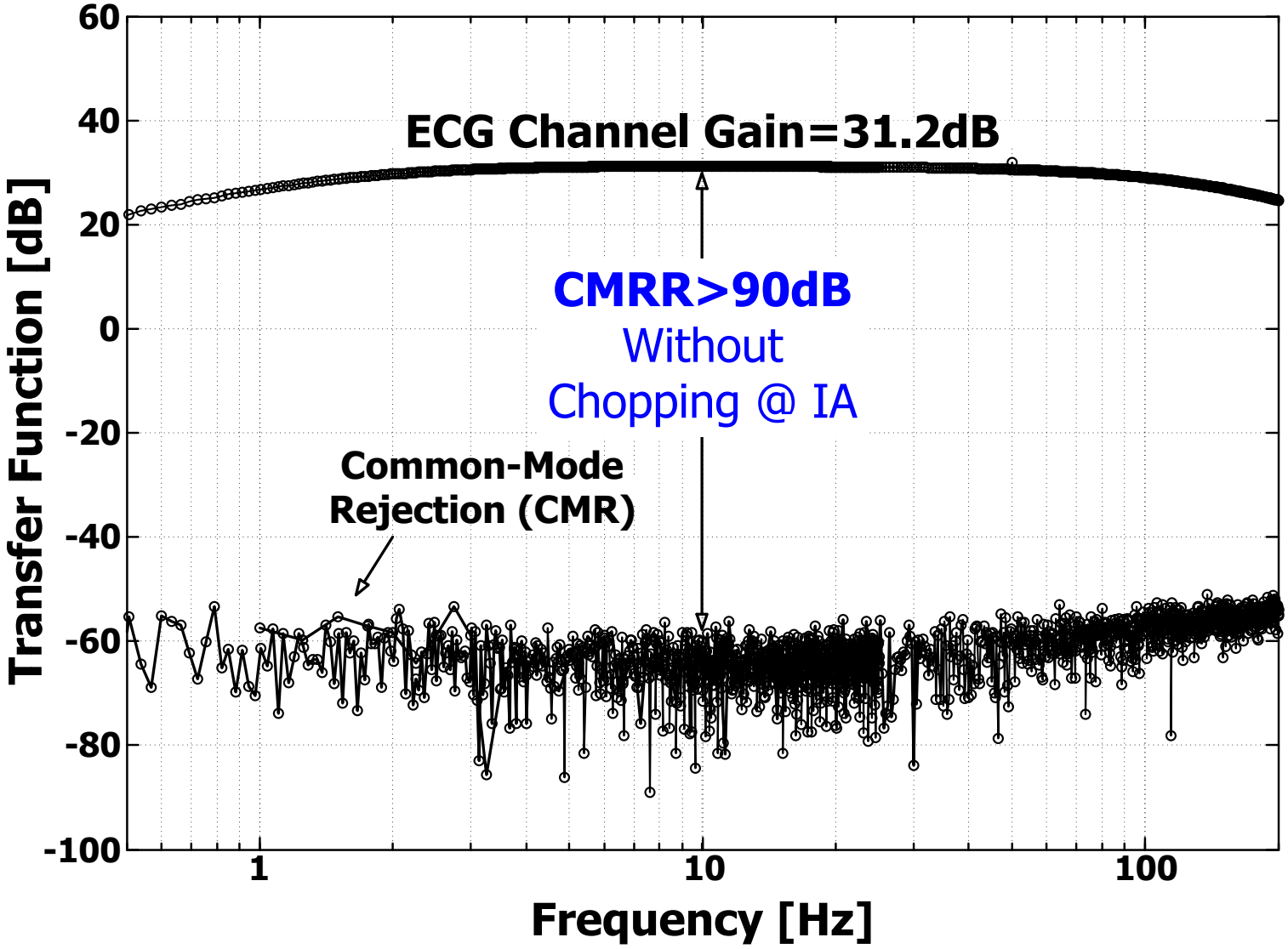
480nV/√Hz @ 20Hz

4.9μV$_{rms}$ @ (1-130Hz)

$$\mathbf{SNR_{in,\ Max.}} = 20*\log10\{V_{in,max}/(V_{n,in}*6.6)\} = \mathbf{70.6dB}$$

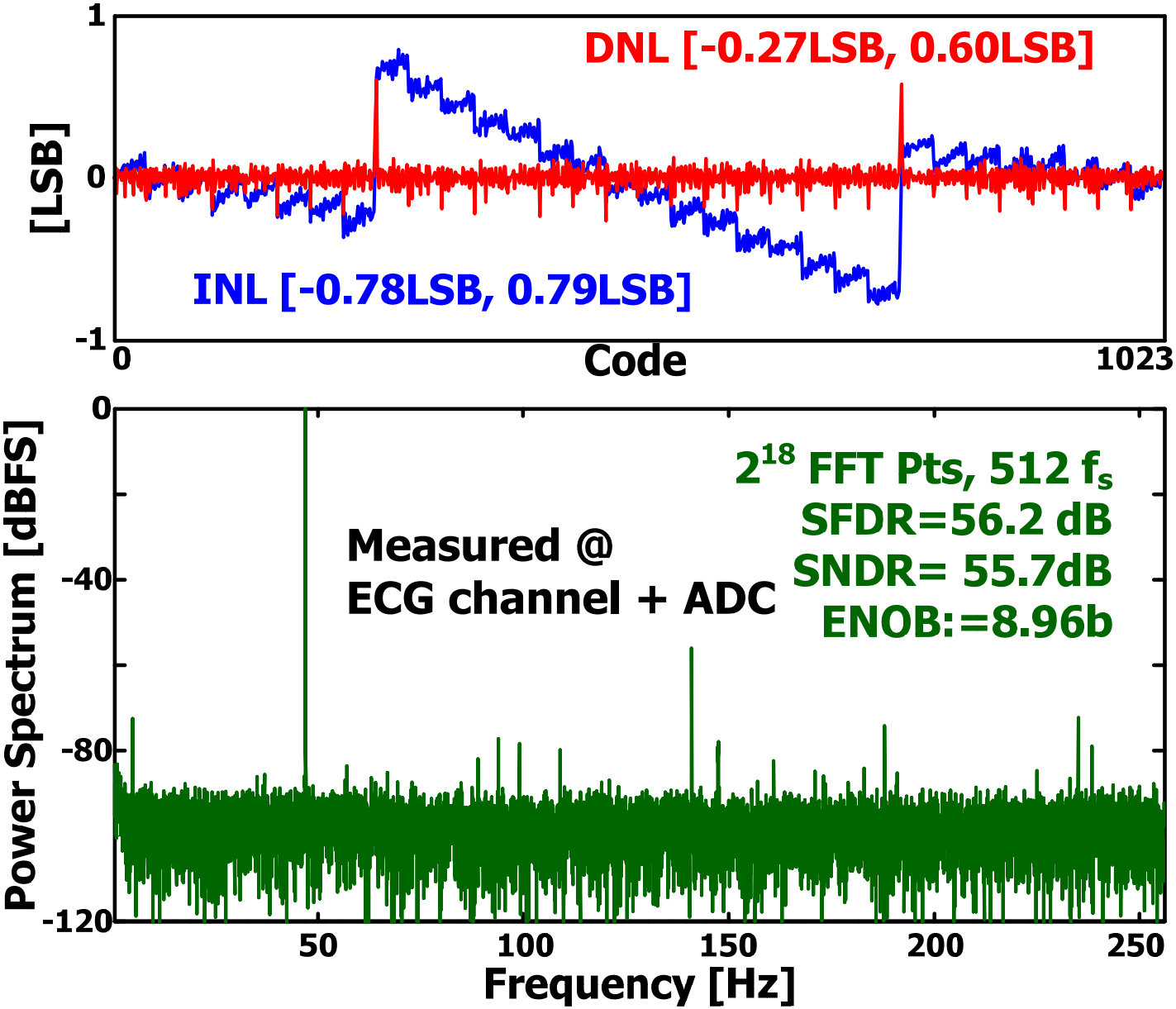
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Common-Mode Rejection Ratio > 90dB



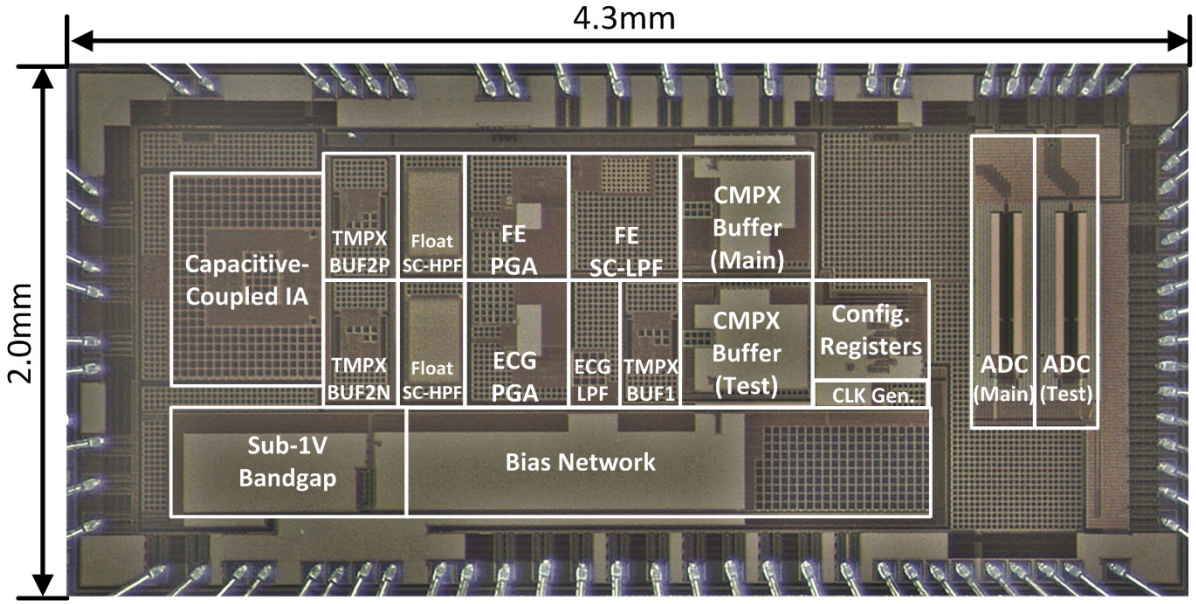
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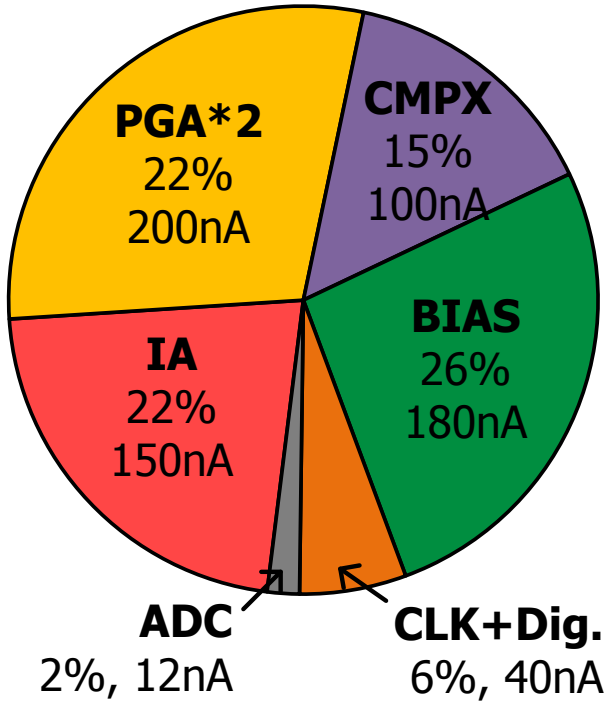
Measurements @ 10b Mode



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ASIC Overview





- 2.0mm x 4.3mm, 180nm CMOS
 - 1P6M, 8kA TM, 2fF/μm^2 MIM, HRI
- 76 bondpads (55 test pins)
- Power: 680nA @ 1.3 - 1.8V Supply (Core & I/O)
- Temperature: 10 - 45^oC

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Performance Comparison

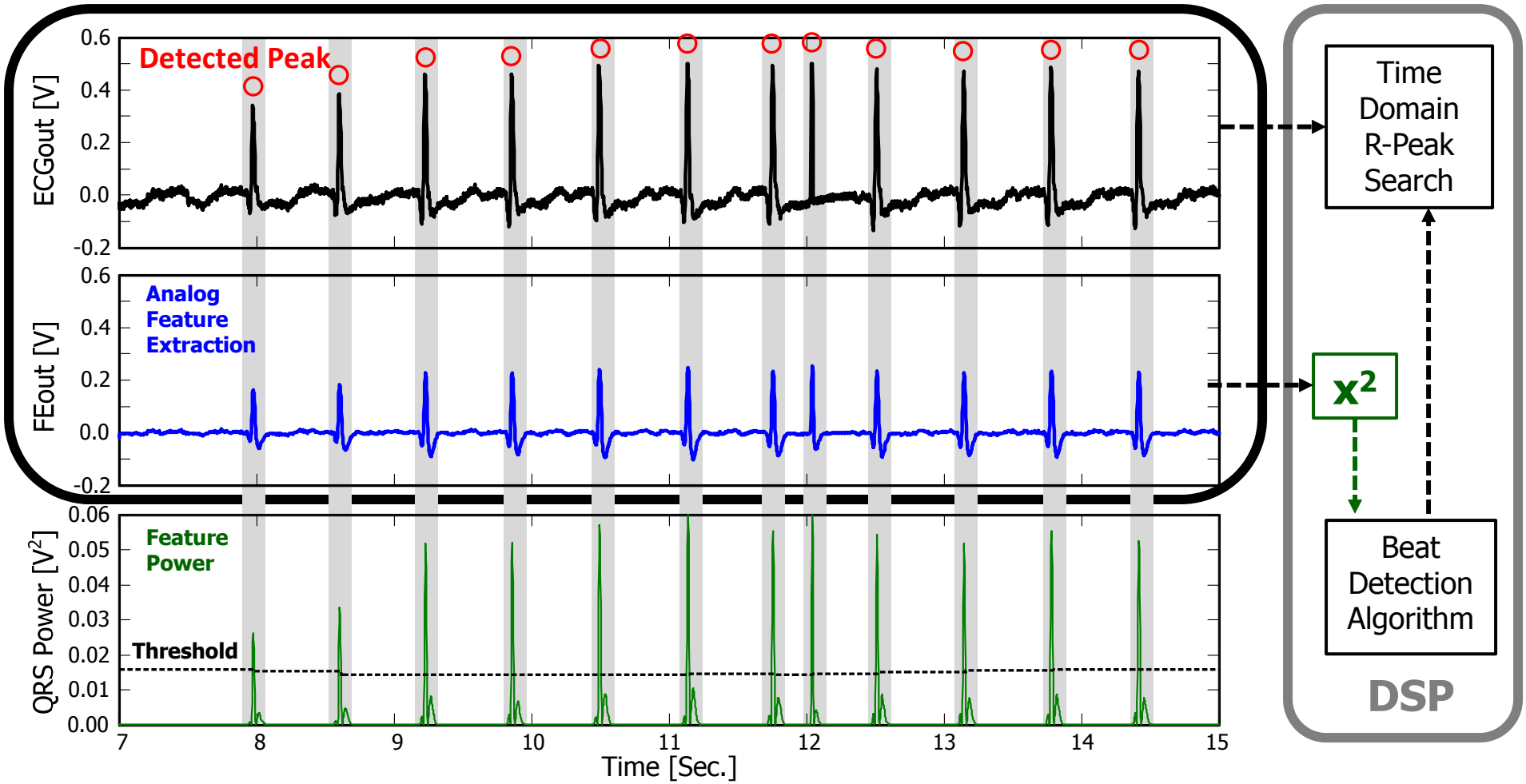
	This Work	[2] ISSCC'13	[3] ISSCC'10	[4] VLSI'10	[5] ISSCC'10	[6] ISSCC'13
Tech. & Supply	**0.18μm 1.3V-1.8V**	0.18μm, 1.7V-1.9V	0.5μm, 2.0V	0.18μm, 0.6V	0.35μm, 1.0V	0.18μm, 0.45V
Current /Channel	**680nA @512S/s/CH**	*8550nA @256S/s/CH	*6900nA @64-1kS/s/CH	*4700nA @ 10kS/s/CH	690nA @312.5S/s/CH	*2118nA @ 2kS/s/CH
Ext. Passives	**No**	Yes	Yes	Yes	Yes	N/A
CMRR/PSRR	**90dB/80dB**	100dB/90dB	105dB	70.4dB	83.2dB/75dB	73dB/80dB
$V_{in,max}$ @ (THD<1%)	**110mV$_{p-p}$**	60mV$_{p-p}$	35mV$_{p-p}$	8mV$_{p-p}$	1mV$_{p-p}$	N/A
Vn,in	**4.9μVrms (130Hz)**	2μVrms (100Hz)	1.1μVrms (170Hz)	3.4μVrms (156Hz)	1.15μVrms (150Hz)	3.2μVrms (10kHz)
SNR_{in}	**70.6dB	73.2dB	73.7dB	51.9dB	42.4	N/A
Resolution	**7-10b**	10b	11b	9b	10b	10b
Analog QRS Extraction	**Yes**	Yes	Yes	No	No	No

* Calculated from the performance reported, ** $SNR_{in}=20*\log10\{V_{in,max}/(V_{n,in}*6.6)\}$

[2] S. Kim, *ISSCC Dig. Tech. Papers*, pp. 302-303, 2013.
[3] R.F. Yazicioglu, *ISSCC Dig. Tech. Papers*, pp.124-125, 2010.
[4] M. Yip, *Symp. VLSI Circuits*, pp. 66-67, 2010.
[5] X. Zou, *ISSCC Dig. Tech. Papers*, pp.126-127, 2010.
[6] D. Han, *ISSCC Dig. Tech. Papers*, pp. 290-291, 2013.

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Heart beat Detection using ASIC

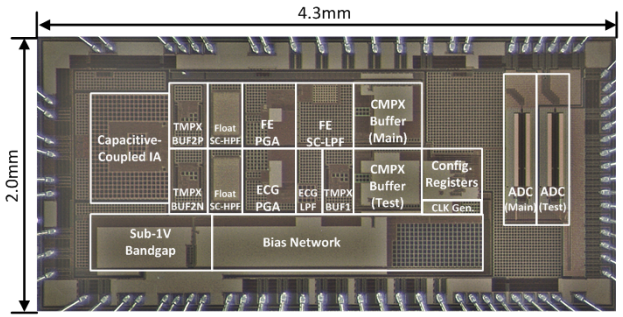


- Analog Feature Extraction is used to extract QRS of ECG signals
- Feature Power is used as input for detection QRS complex
- Detected beat is referred to time-domain ECG signals to find R-peak

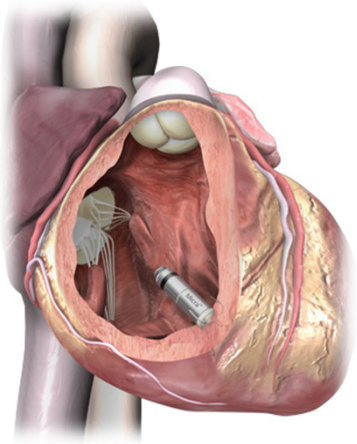
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Conclusions

- Ultra-low power implantable ECG acquisition IC
 - Highly integrated solution
 - ➔ No external passives, a few digital configurations
 - ➔ Analog Feature Extraction
 - 680nA power consumption, 10b dynamic range
- The ASIC will benefit the future miniature pacemaker







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ISSCC 2014

A 0.5V 1.27mW Nose-on-a-Chip for Rapid Diagnosis of Ventilator-Associated Pneumonia

K.-T. Tang[1], S.-W. Chiu[1], C.-H. Shih[2], C.-L. Chang[1], C.-M. Yang[1], D.-J. Yao[1], J.-H. Wang[1], C.-M. Huang[1], H. Chen[1], K.-H. Chang[1], C.-C. Hsieh[1], T.-H. Chang[1], M.-F. Chang[1], C.-M. Wang[1], Y.-W. Liu[1], T.-J. Chen[3], C.-H. Yang[3], H. Chiueh[3], J.-M. Shyu[1]

[1]National Tsing Hua University, Hsinchu, Taiwan

[2]Taipei Medical University, Taipei, Taiwan

[3]National Chiao Tung University, Hsinchu, Taiwan

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Outline

1. Introduction of Ventilator-Associated Pneumonia (VAP)
2. Gas Detection for VAP Diagnosis
3. Nose-on-a-Chip
4. Chip Measurement and Clinical Results
5. Conclusions

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Ventilator-Associated Pneumonia



- Infection
- Medication
- Sputum Culture
- T → Alleviation
- F → Change Medication

- High probability to receive VAP in ICU
 - Mortality rate: 20-50%
- Routine Procedure
 - Examination
 - Antibiotics

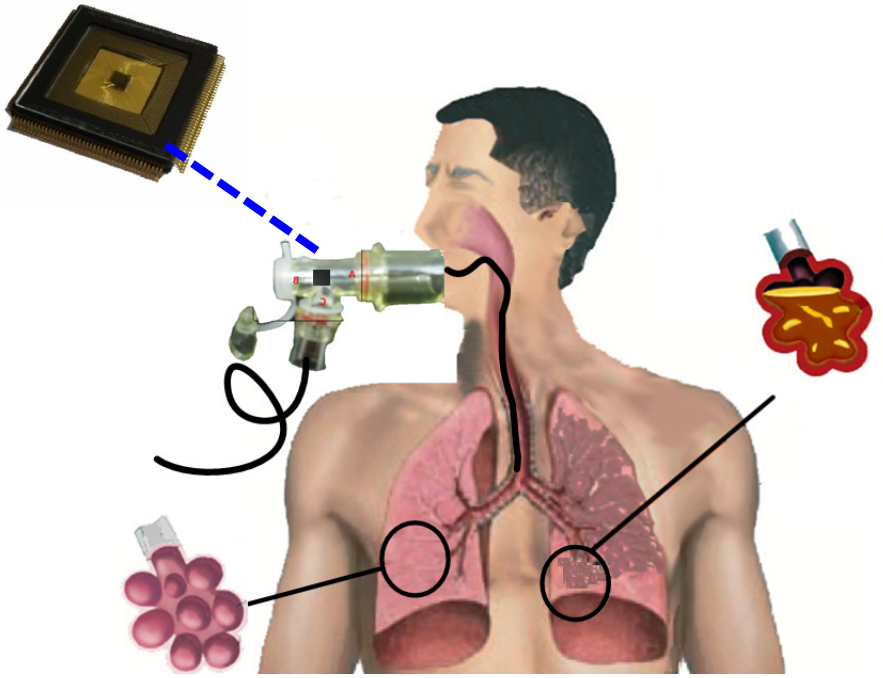


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Gas Detection for VAP Diagnosis

- Chest physician
 - Rapid & accurate diagnosis
- Gas analysis method
 - Special smell from patients
- VAP diagnosis chip
 - Gas detection
 - Integrated with ventilator
 - Personal use
 - Real-time monitoring
 - Robust classification

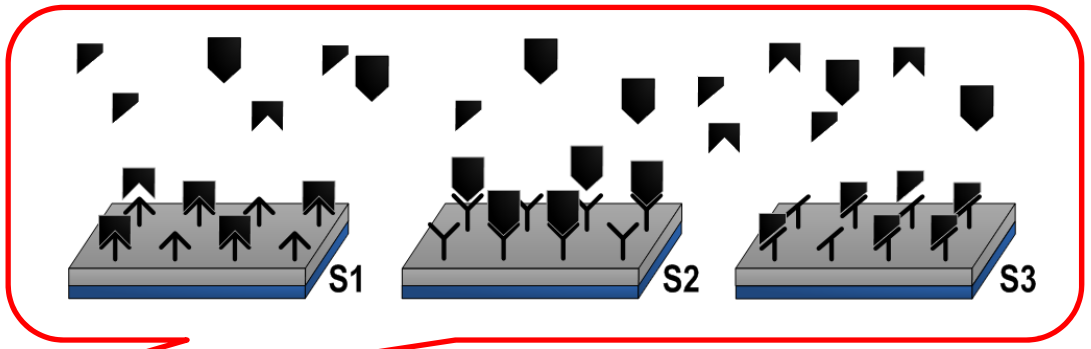
VAP Diagnosis Chip

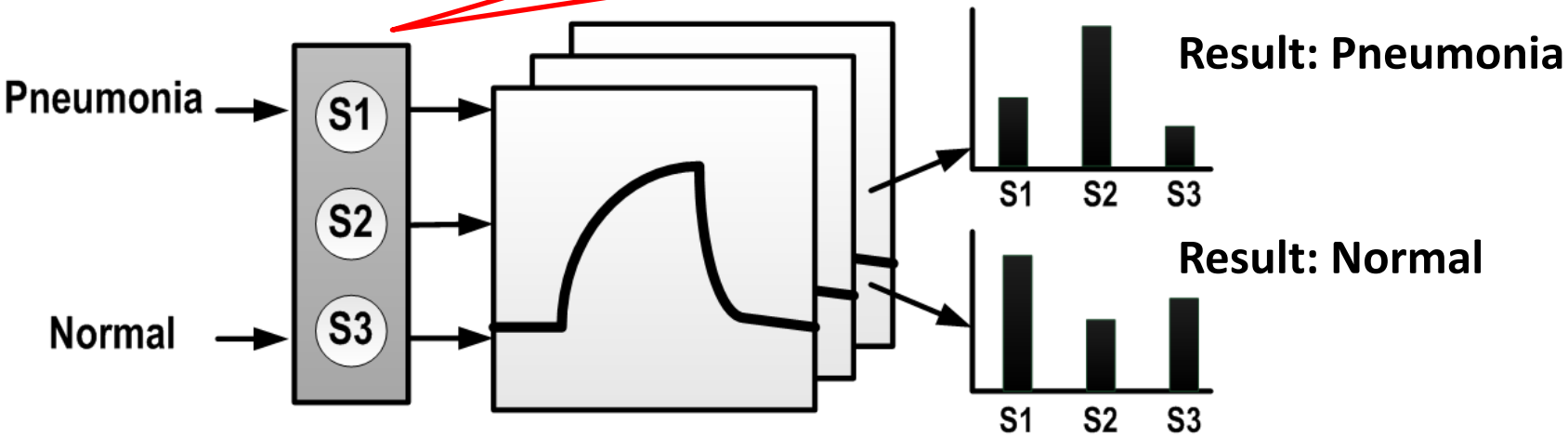


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Principle of Electronic Nose

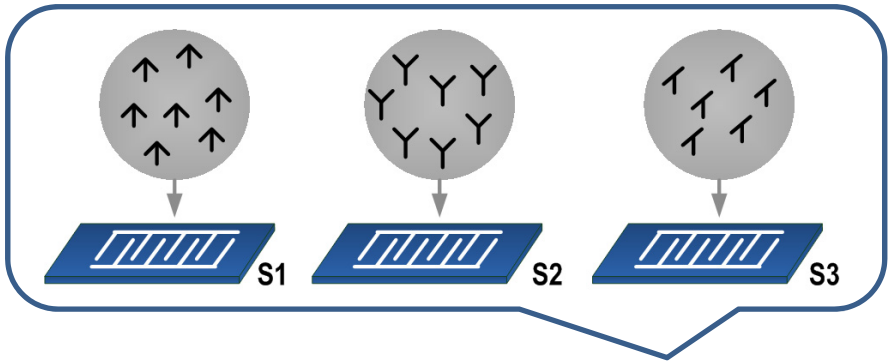
- Bio-mimetic olfactory system, electronic nose (e-nose)
- Compared to GC-MS, e-nose has the potential to be
 - Small
 - Fast
 - Inexpensive
 - Easy to operate



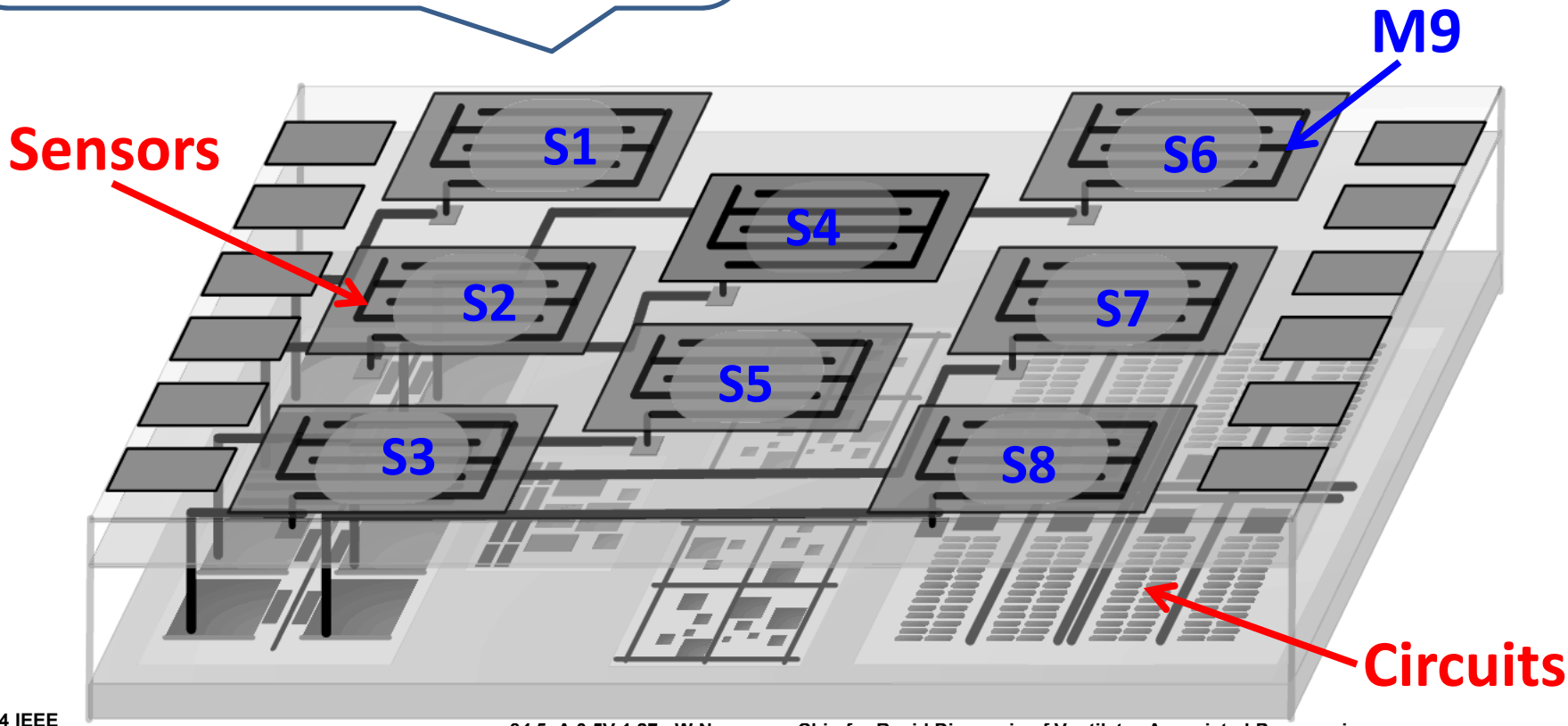


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Nose-on-a-Chip

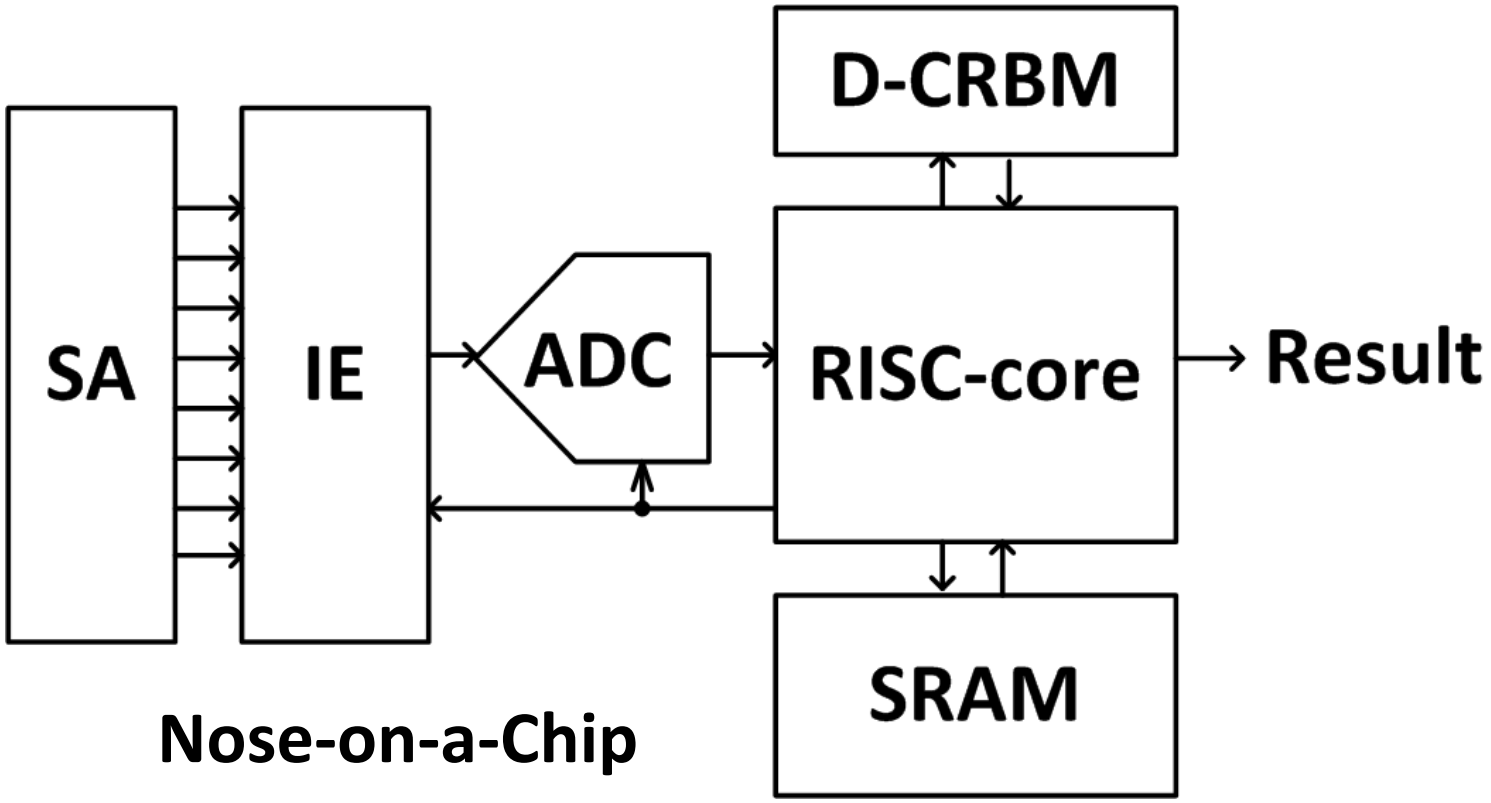


- Standard CMOS Process
- Fully Integration
- Room temperature



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System Block Diagram



Nose-on-a-Chip

- Sensor Array (SA)
- Interface Circuit (IE)
- 10b SAR ADC
- RISC-core (OR1200)
- Digital (D-)CRBM
- SRAM

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VAP in Vitro Experiment

- Collect the most common ten kinds of bacteria
 - *E. coli, Klebsiella Oxytoca, Acinetobacter Baumannii, Klebsiella Pneumoniae, Stenotrophomonas Maltophilia, Proteus Mirabilis, Enterobacter Aerogenes, Enterobacter Cloacae, Pasteurella Multocida, Staphylococcus Aureus*
- Bacterial culture
 - 1000ml sample bag
 - 5% CO_2, 95% air
 - Incubator at 37 degree C
- Analysis with GC-MS

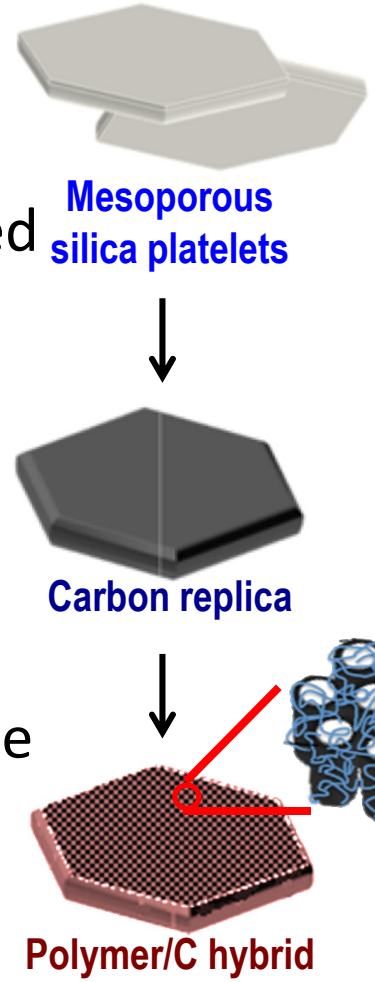
Carbide, Sulfide, Ammonia

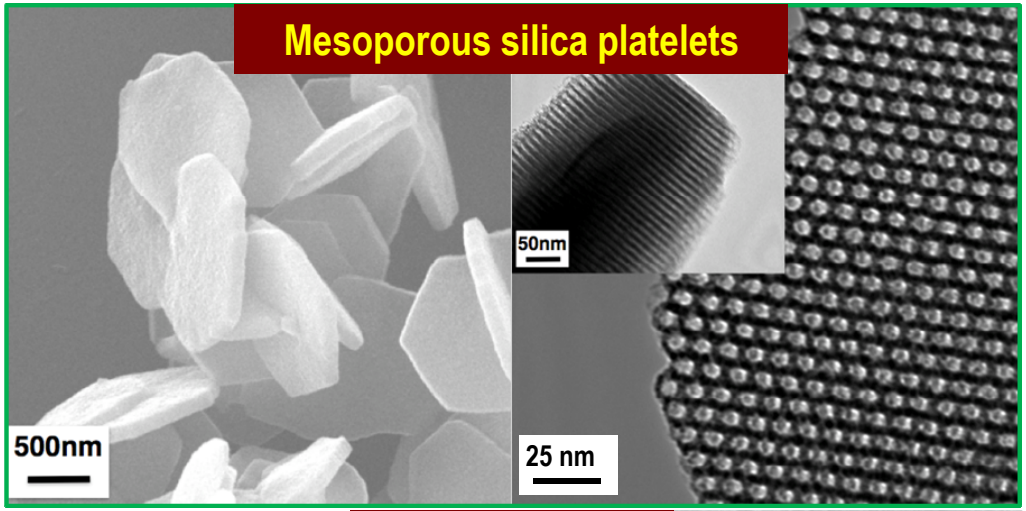


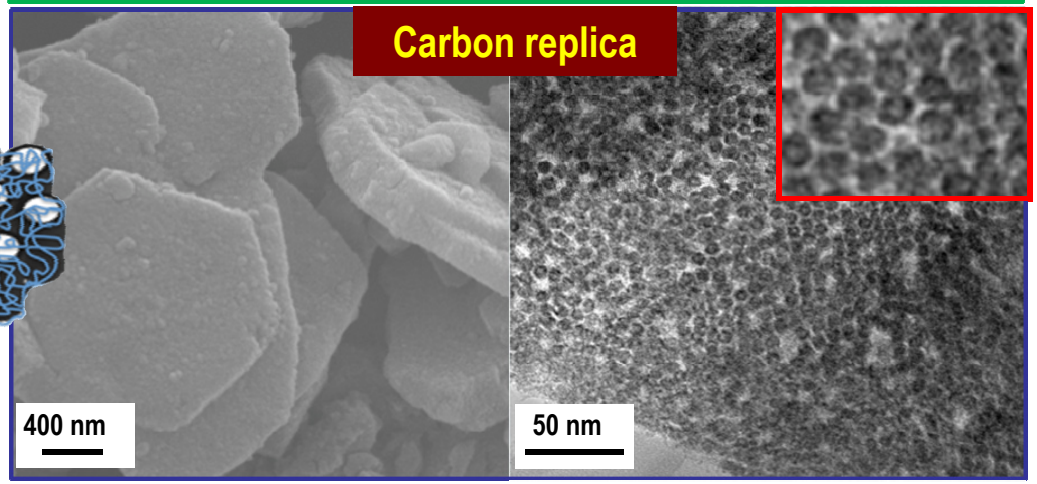
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Mesoporous Carbon Preparation

- Platelet-shaped mesoporous SBA-15 silica
- Polymers are grown onto the carbon





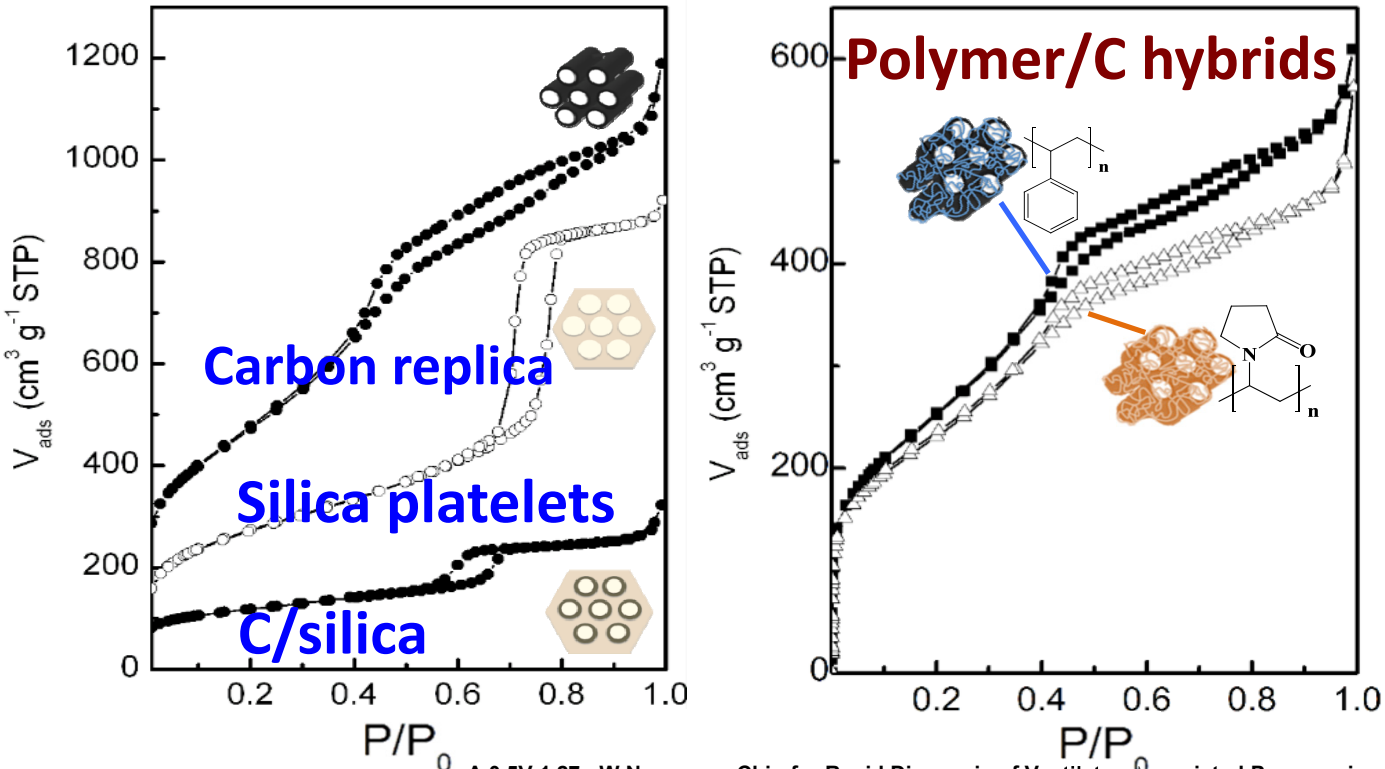


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High Gas Sensitivity

- High surface areas
- Large pore volumes
- Relatively uniform mesoporosity

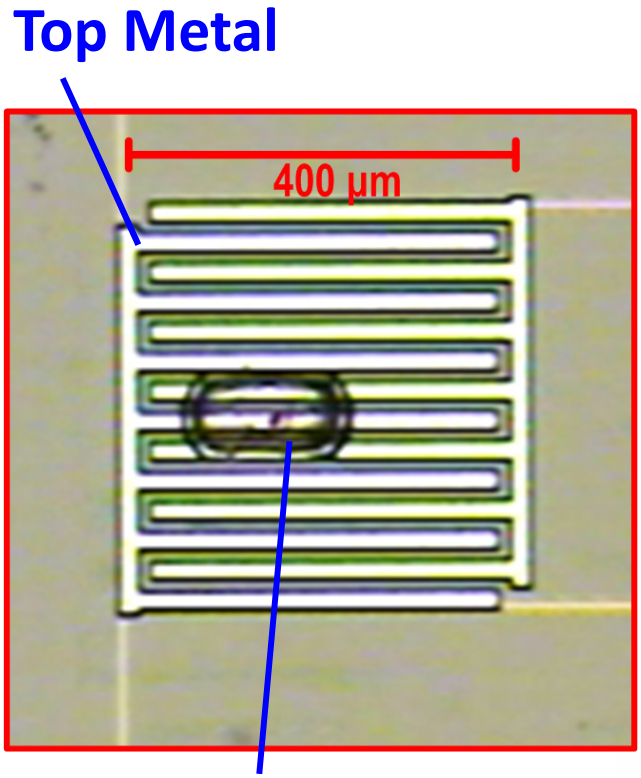
Nitrogen physisorption analysis

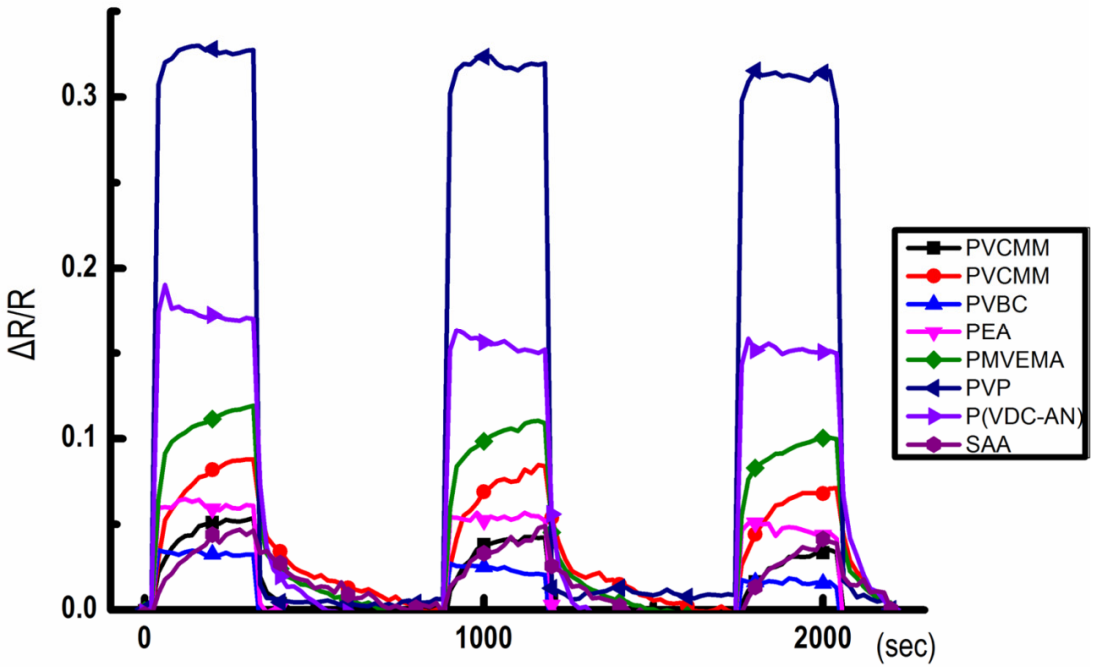


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Sensor Array

- Interdigital electrodes: Metal 9 (top metal)
 - Area: 400 × 400 μm^2
 - Exposed area: defined by PAD Mask

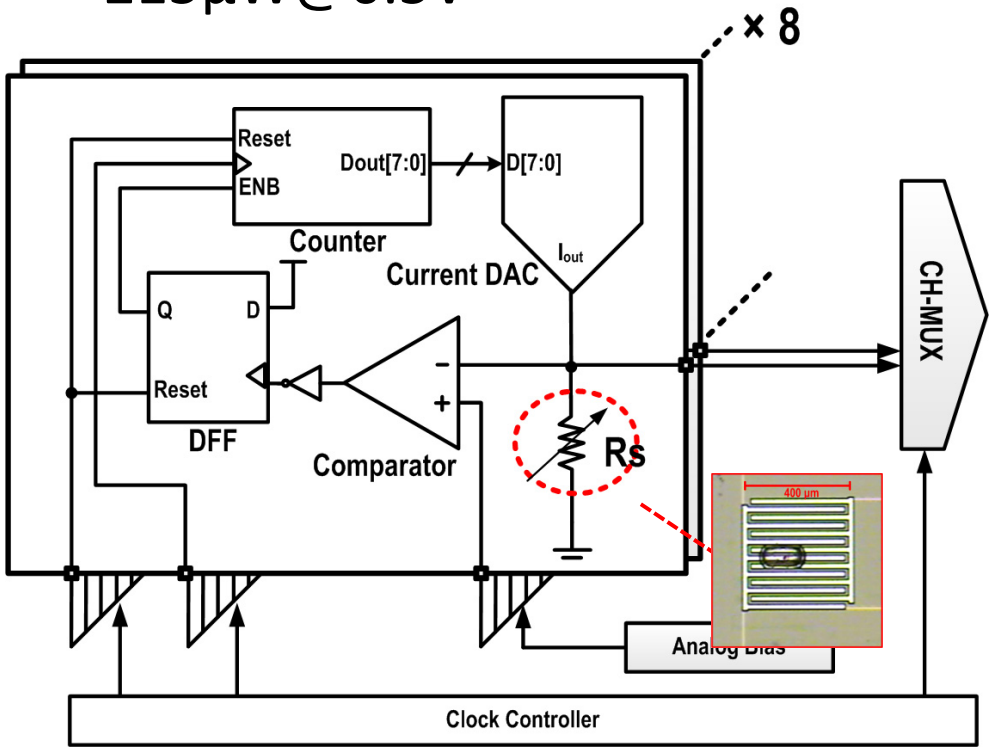


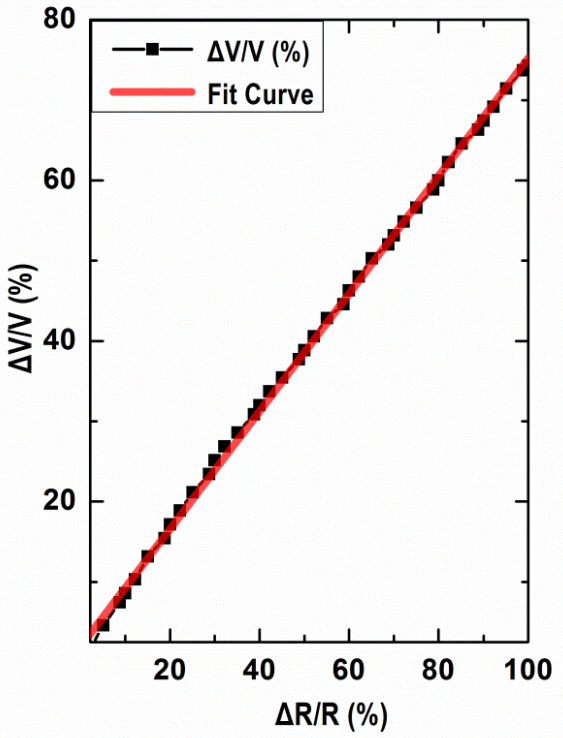


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Interface Circuit

- "Adaptive" to reduce the baseline drift variation
 - Temperature, humidity, background odors
- 8-channel adaptive interface
 - 215µW@0.5V

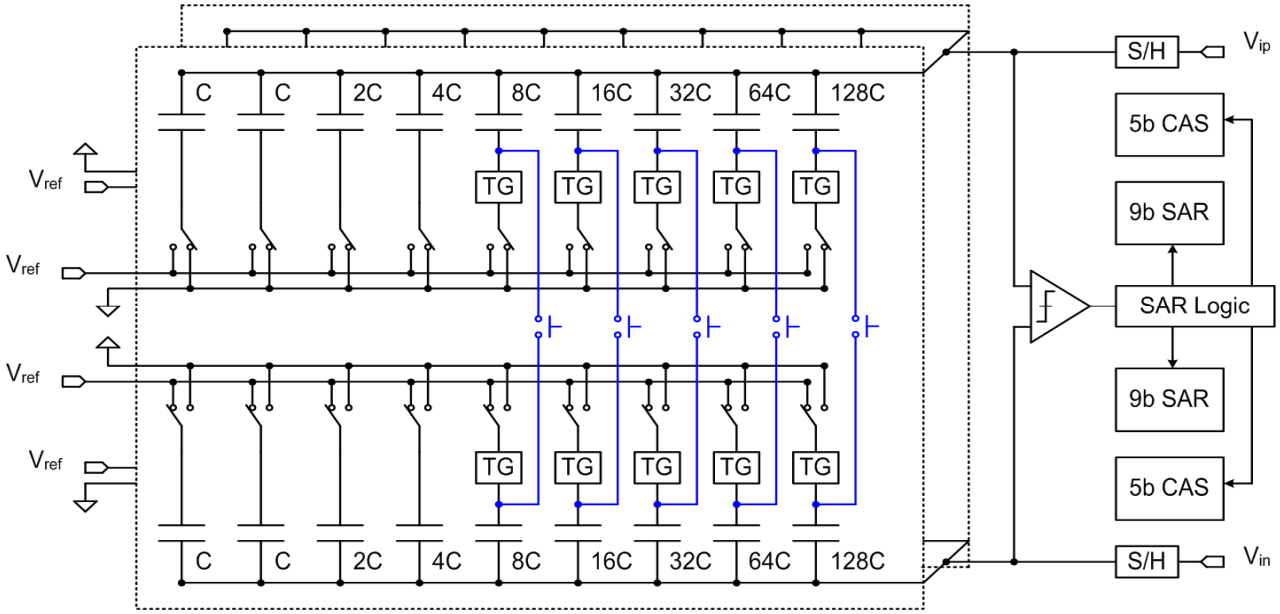




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10b SAR ADC

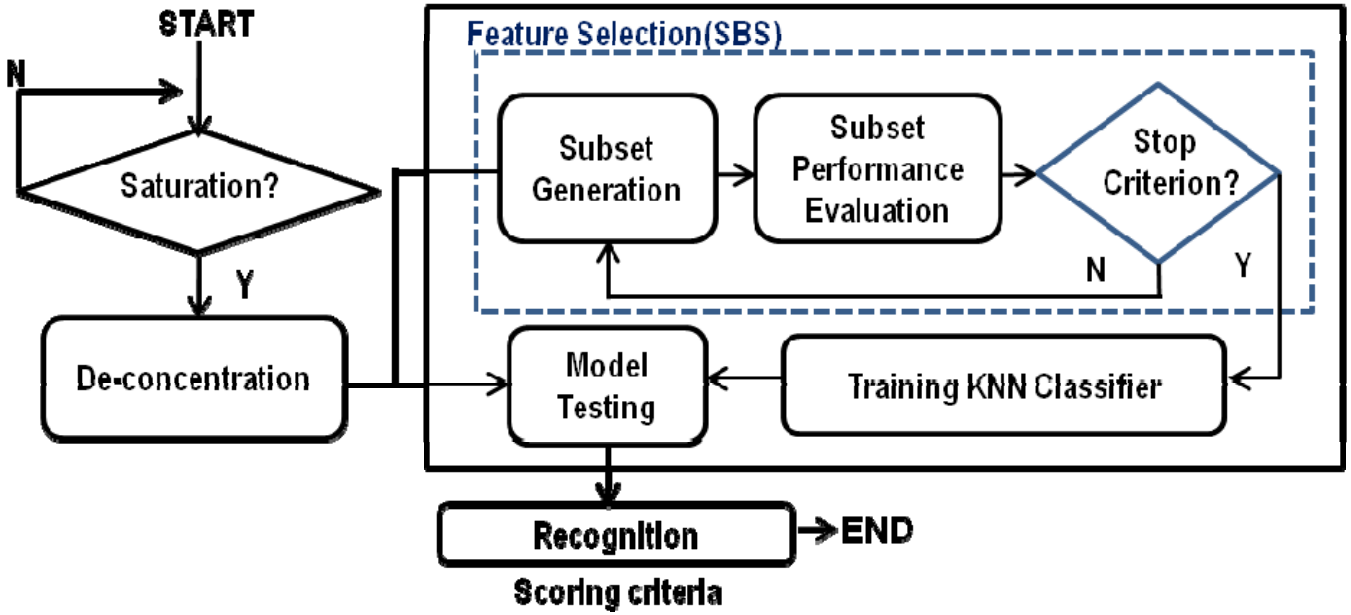
- Charge-average switching (CAS) [1] [ISSCC 2013, NTHU]
 - Minimize the disturbance and noise of the reference supply voltage
 - Reduce the switching energy to 88.6 CV_{ref}^2 (48% saving)
 - Cost 1.15μW@0.5V



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RISC-core

- RISC-core Processor (OpenRISC1200)
 - Sensor saturation, signal normalization
 - Sequential backward selection (SBS) scheme
 - K-Nearest Neighboring (KNN) classifier



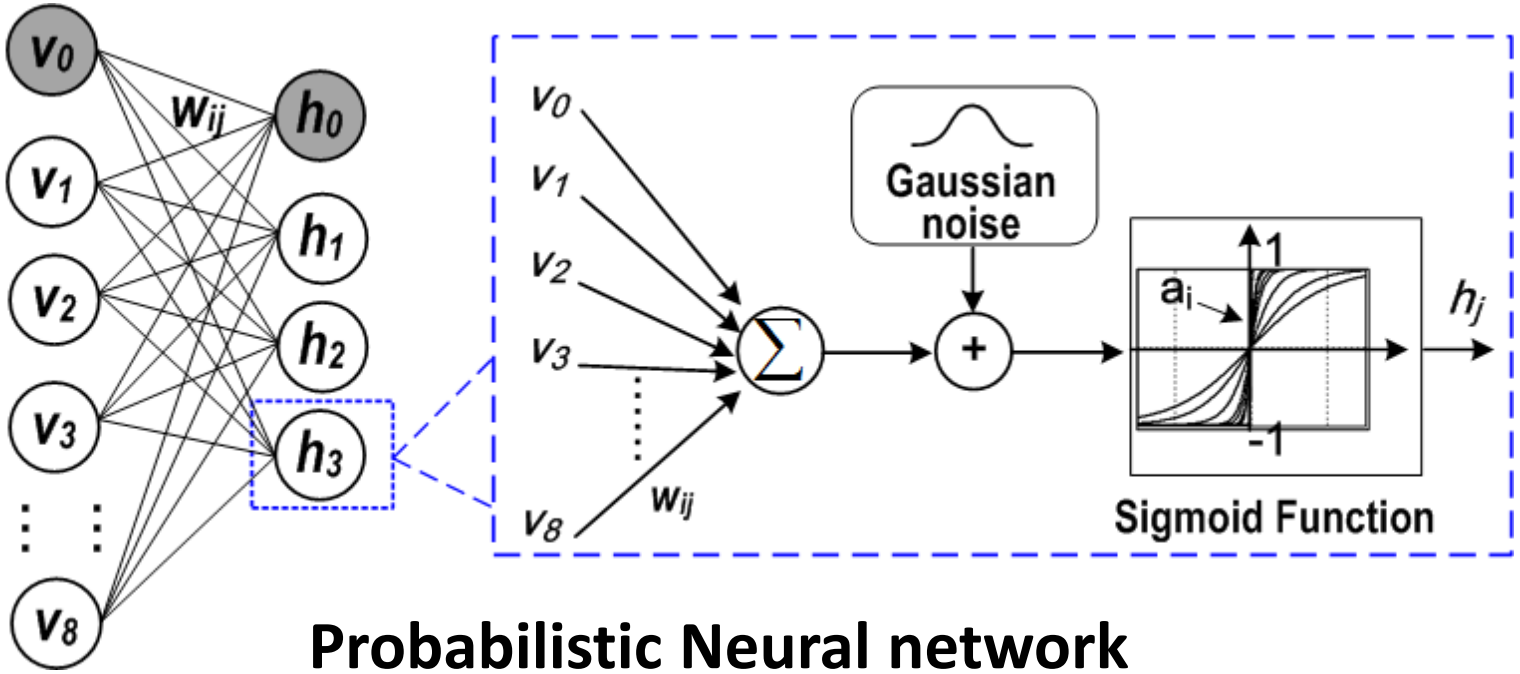
Detection	
W/o SBS	W/ SBS
74.3%	**85.6%**

Bacteria	
W/o SBS	W/ SBS
76.4%	**91.8%**

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Digital (D-)CRBM

- Continuous Restricted Boltzmann Machine (CRBM) [2]
 - Data clustering
 - Dimension reduction
 - Enlarge differences
 - Import probability noise
 - Suitable for complex gas
 - Overcome the variation

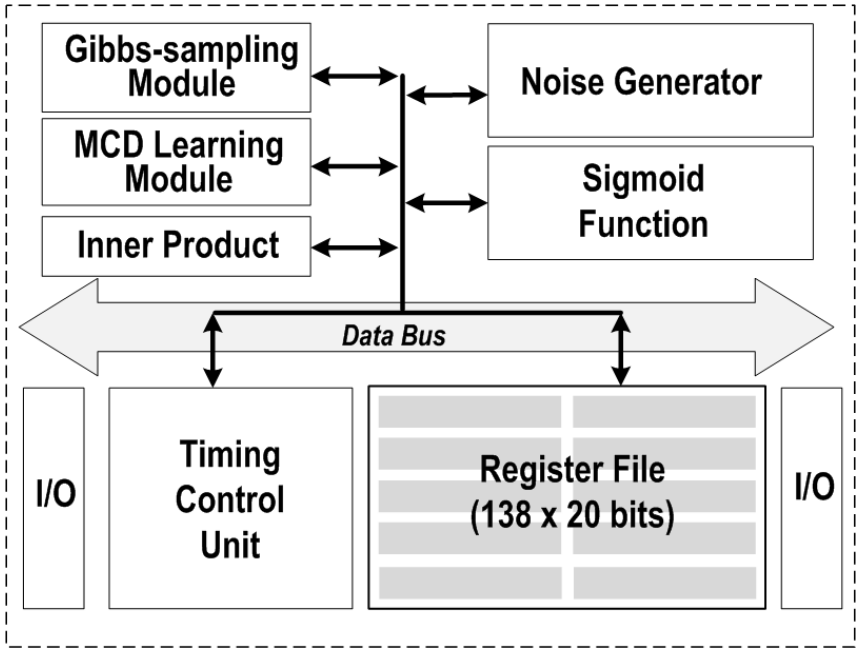


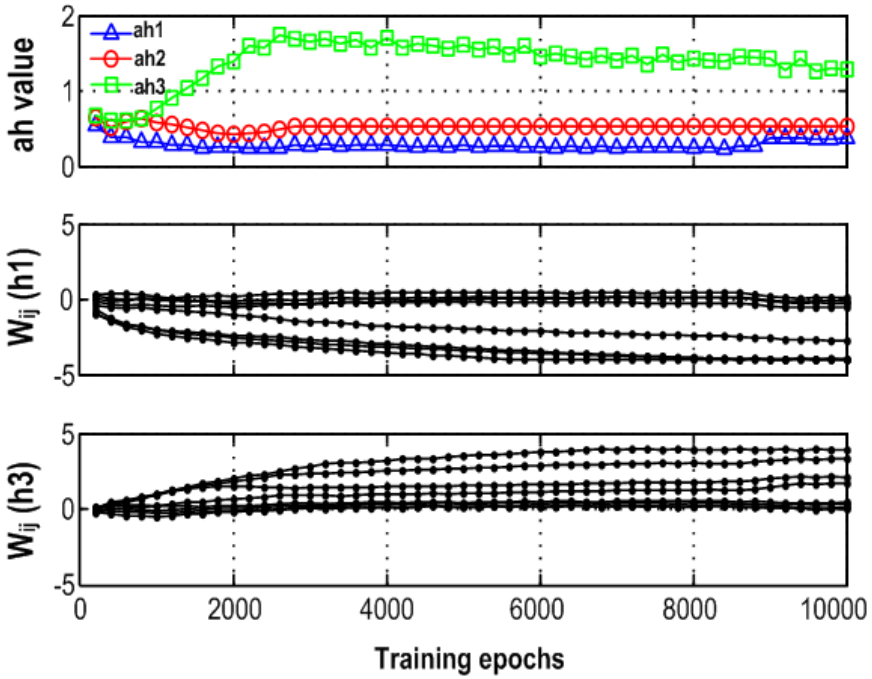
Probabilistic Neural network

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D-CRBM Learning

- Digital approach implementation
- The learning trajectories: 5,000 training epochs
- The hidden neurons of the trained CRBM respond differently to sensory data

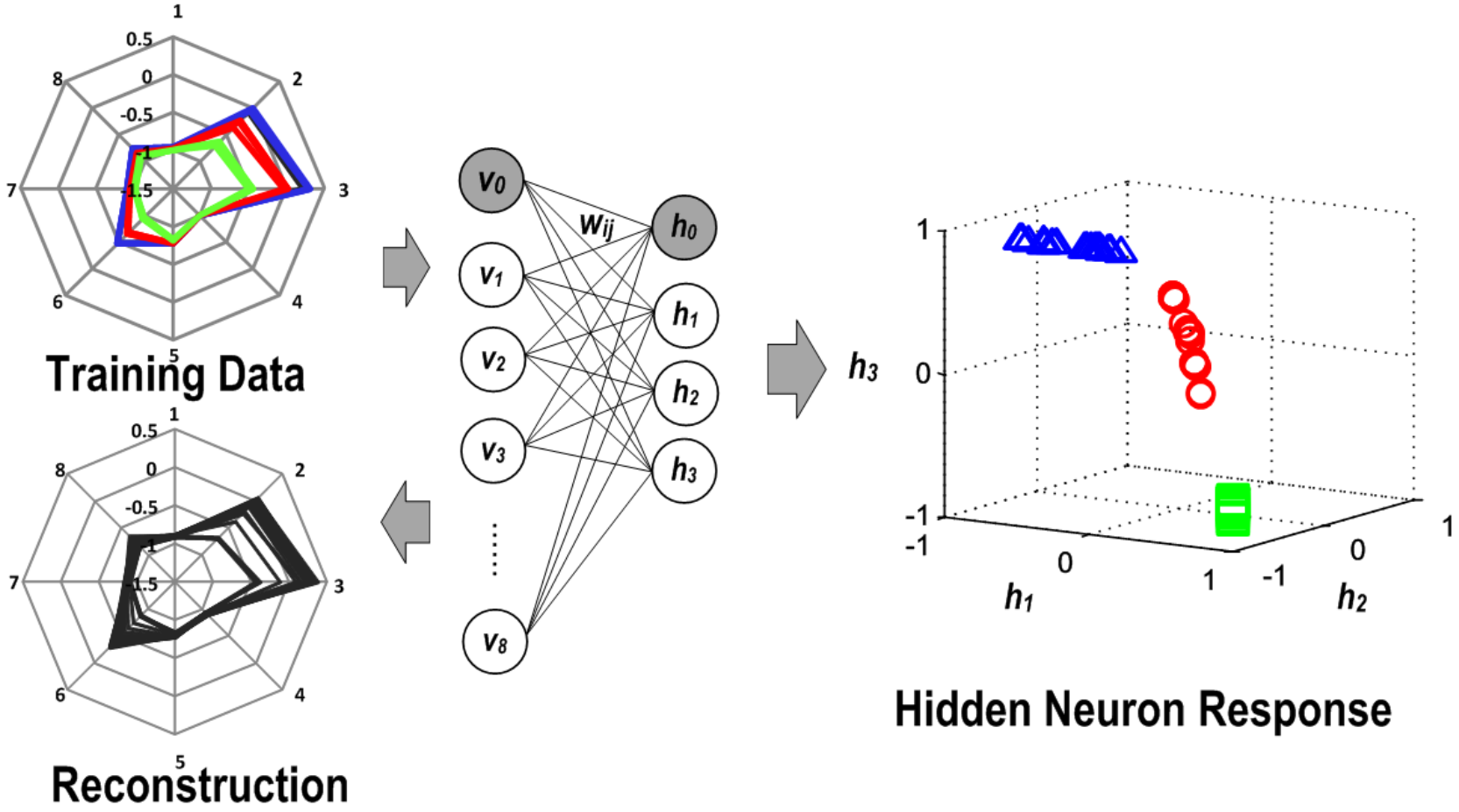




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D-CRBM Reconstruction

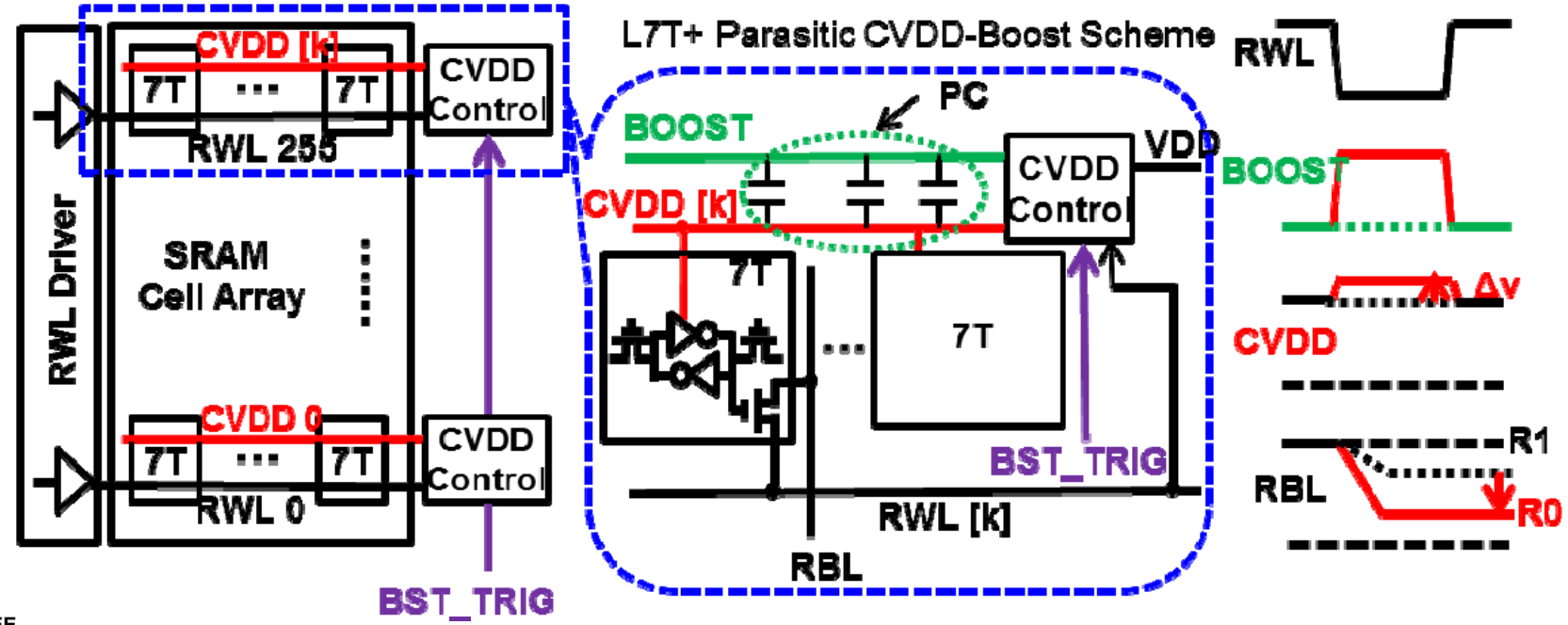
- Reconstruction vs. Training data



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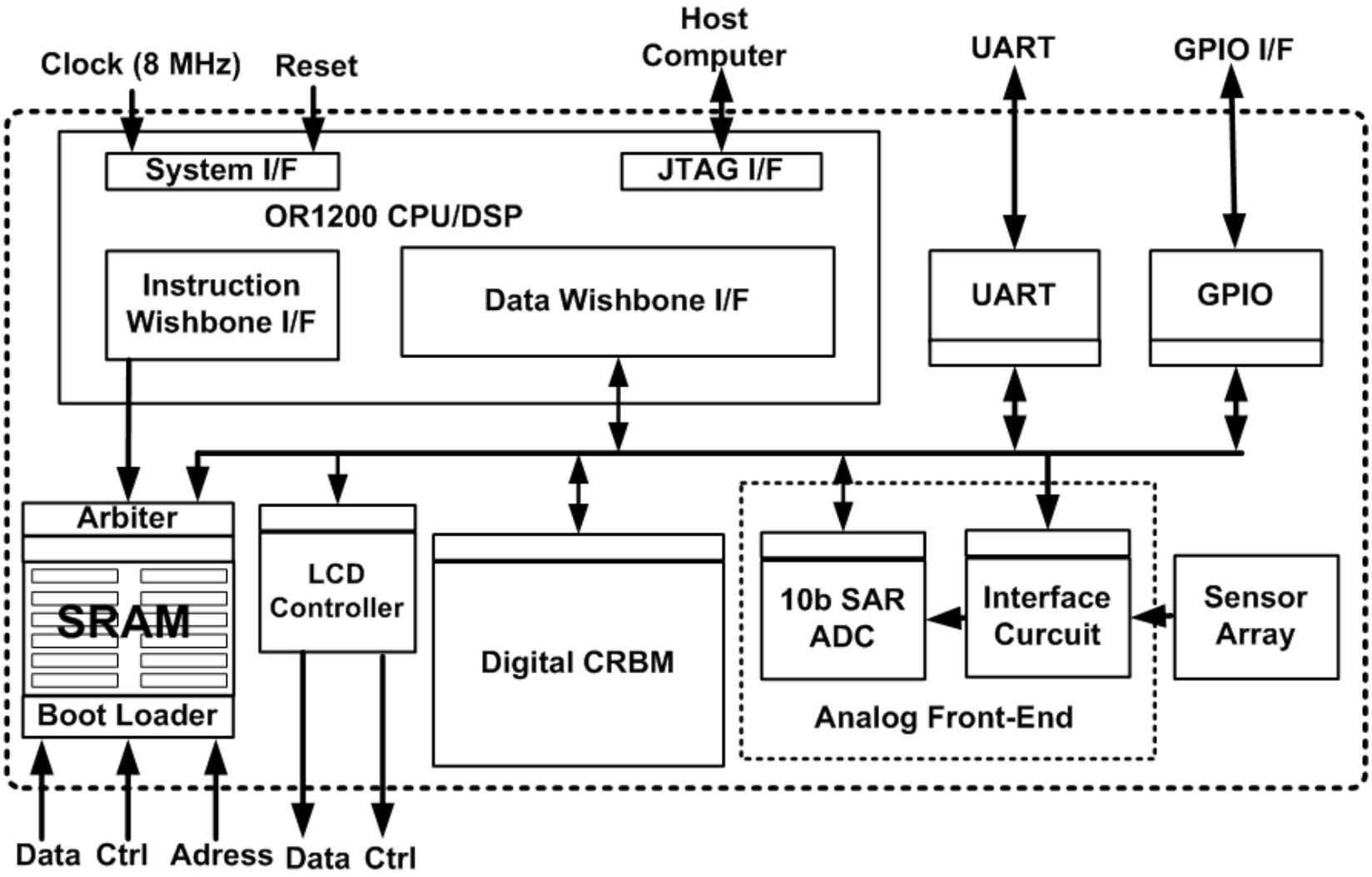
Low VDDmin SRAM

- Read-Disturb-Free 7T SRAM cell (L7T cell) [3]
 - 1T read-decoupled read-port (RP) [VLSI Symp. 2012, NTHU]
- Parasitic CVDD Boost
 - Increase cell current and RBL voltage swing (for Read-0)
 - Lower VDDmin and faster read speed



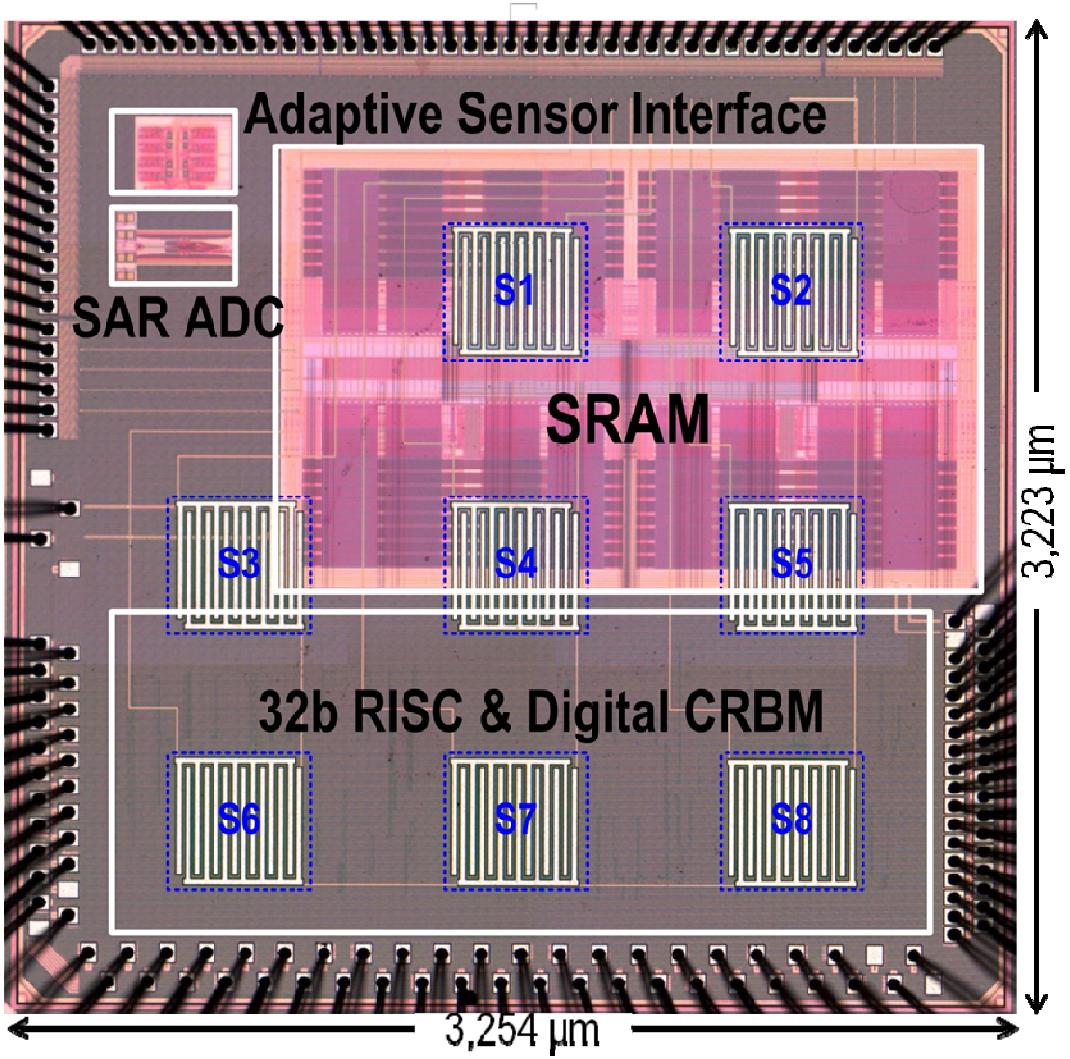
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Complete System Block Diagram



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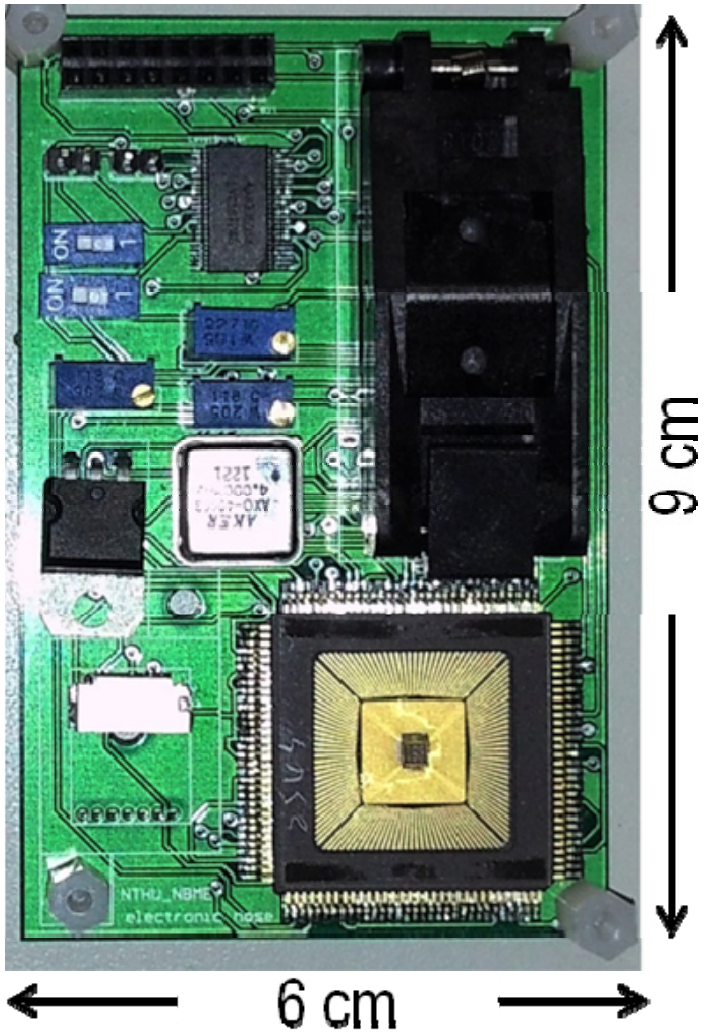
Chip Micrograph



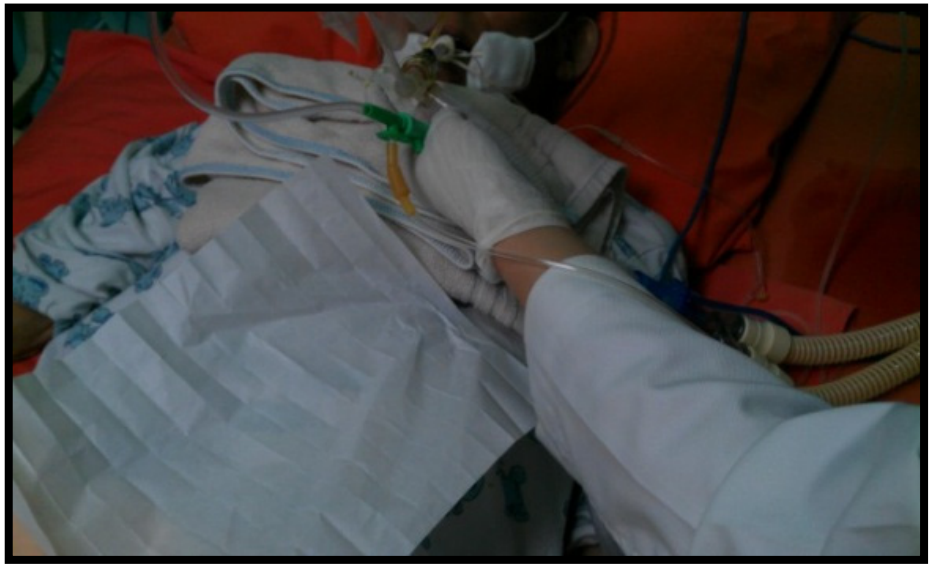
Chip Summary	
Technology	1P9M 90nm CMOS
Die Size	10.49 mm^2
Supply Voltage	0.5V
Power Dissipation	1.27mW
Frequency	8MHz
Sub-Blocks	
On-Chip Sensors	8 Polymer-Carbon Composites
Adaptive Interface	8 Channels, Range: 5k - 100kΩ
SAR-ADC	10b
Processor	32b RISC
SRAM	L7T, 8Kx32b
Learning Kernel	CRBM

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Prototype and Clinical Trial



VAP Patient







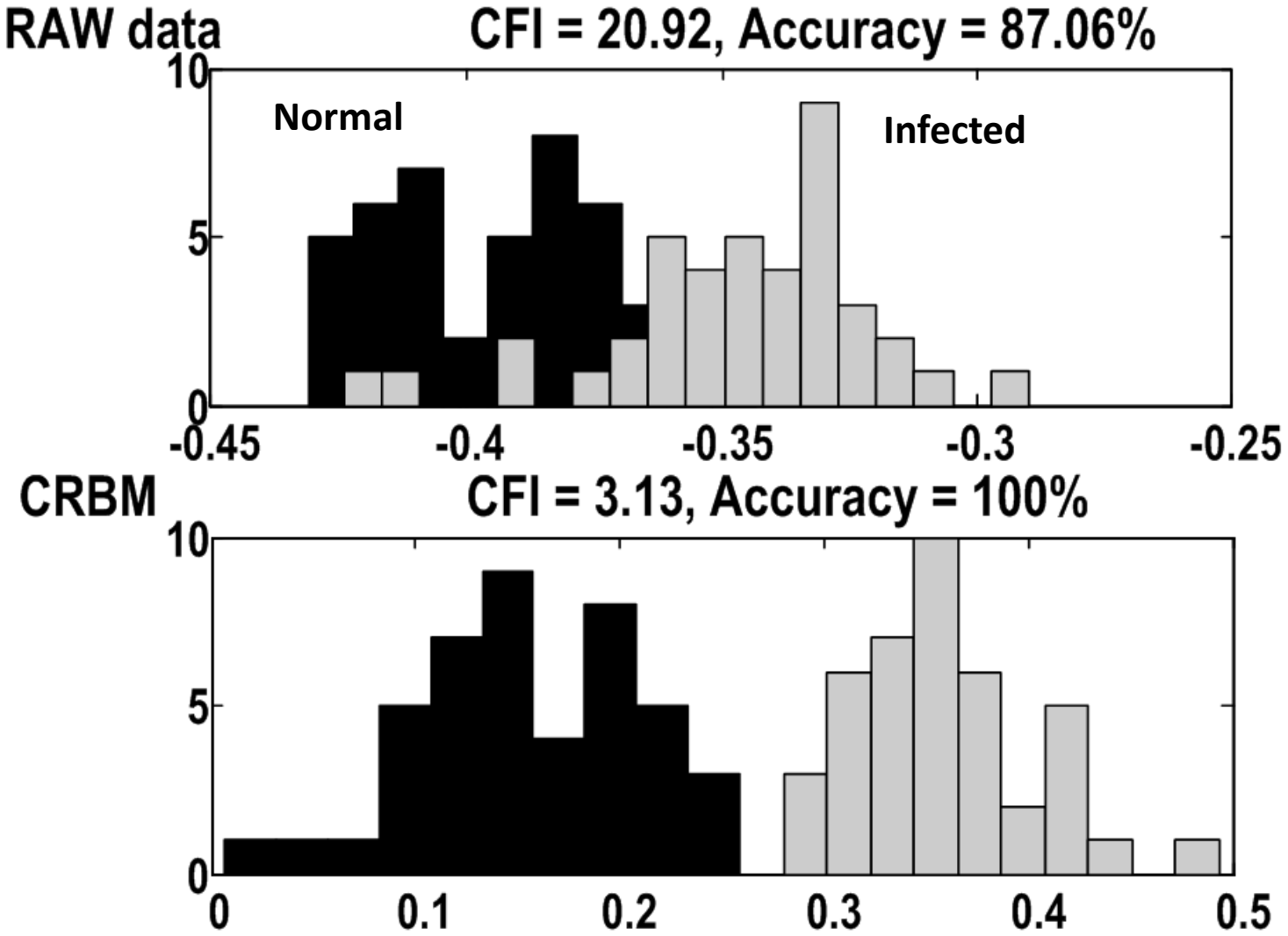
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Pneumonia Identification

- 117 samples taken
 - Experimental group: 74 samples infected with pneumonia (35 Klebsiella, 39 Pseudomonas aeruginosa)
 - Control group: 43 Normal patients
- The classification results performed in two steps:
 - 1) Recognizing whether the patient was infected
 - 2) If infected, identifying which microorganism was the source

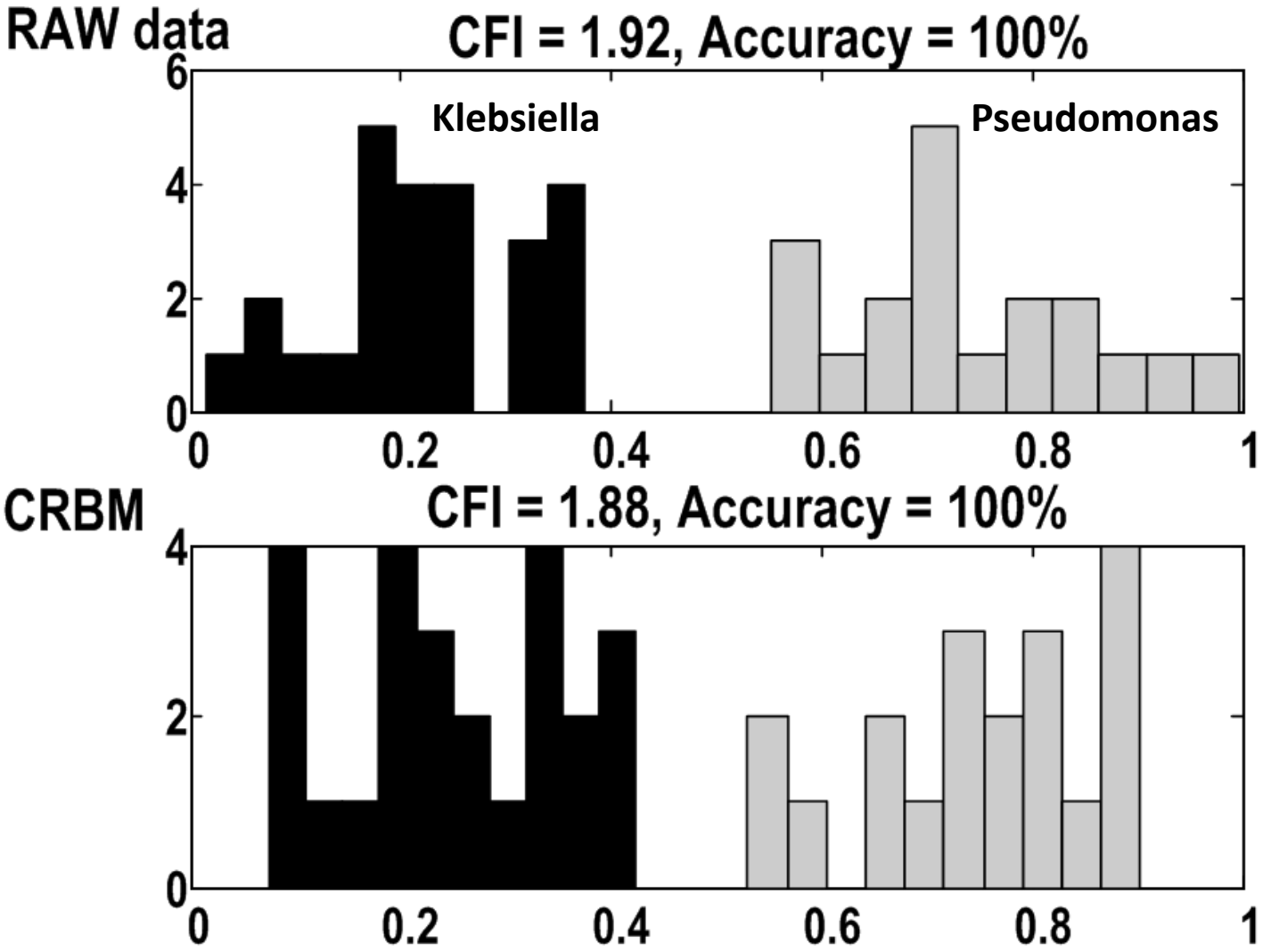
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Normal vs. Infected



Clustering Fisher Index (CFI)

Klebsiella vs. Pseudomonas



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Comparison with Prior Arts

	ISSCC'02 [4]	TBCAS'11 [5]	ISSCC'12 [6]	This Work
CMOS Technology	0.8µm	0.18µm	0.25µm	**90nm**
Supply Voltage (V)	>5	1.8	3.3	**0.5**
Channels	3	8	1	**8**
Power Dissipation (mW)	>7.25	2.81	1.35	**1.27**
On-Chip Sensor	Post-MEMS	-	-	**Standard CMOS**
Sensor Interface	Not Adaptive	Self Adaptive	Not Adaptive	**Self Adaptive**
Embedded Processor	-	8b 8051	-	**32b RISC**
On-Chip Memory	-	6T, 16Kx8b	-	**L7T, 8Kx32b**
Learning Kernel	-	-	-	**CRBM**
Scalability	-	-	-	**YES**

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Conclusions

- Fully-integrated Nose-on-a-Chip for VAP diagnosis
 - First demonstration of fully-integrated SoC for rapid diagnosis of ventilator-associated pneumonia
 - Lowest power dissipation among the state-of-the-art nose-on-a-chips
- Flexible and powerful signal processing capability
 - 32-bit RISC-core with a special gas data processing unit (D-CRBM)
- Successful VAP identification
 - Identify healthy and Infected patient, and further to Klebsiella and Pseudomonas at the success rate of 100%

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Acknowledgements

- National Science Council
- Chip Implementation Center
- Chung-Shan Institute of Technology
- Ministry of Education

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- **Thanks for your Attention!**

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Reference

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- H. Chen, *et al*., “Continuous restricted Boltzmann machine with an implementable training algorithm,” *IEE P-VIS IMAGE SIGN*, pp. 153-158, Aug. 2003.
- M.-B. Chen, *et al*., “A 260mV L-shaped 7T SRAM with Bit-Line (BL) Swing Expansion Schemes Based on Boosted BL, Asymmetric-V_{TH} Read-Port, and Offset Cell VDD Biasing Techniques,” *VLSI Symp.*, pp. 112-113, June 2012.
- C. Hagleitner, *et al*., "A gas detection system on a single CMOS chip comprising capacitive, calorimetric, and mass-sensitive microsensors," *ISSCC*, pp. 430-479, Feb. 2002.
- K.-T. Tang, *et al.*, "A Low-Power Electronic Nose Signal-Processing Chip for a Portable Artificial Olfaction System," *IEEE T BIOMED CIRC S.*, pp.380-390, Aug. 2011.
- V. Petrescu, *et al.*, "Power-efficient readout circuit for miniaturized electronic nose," *ISSCC*, pp. 318-320, Feb. 2012.

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A CMOS Micro-Flow Cytometer for Magnetic Label Detection and Classification

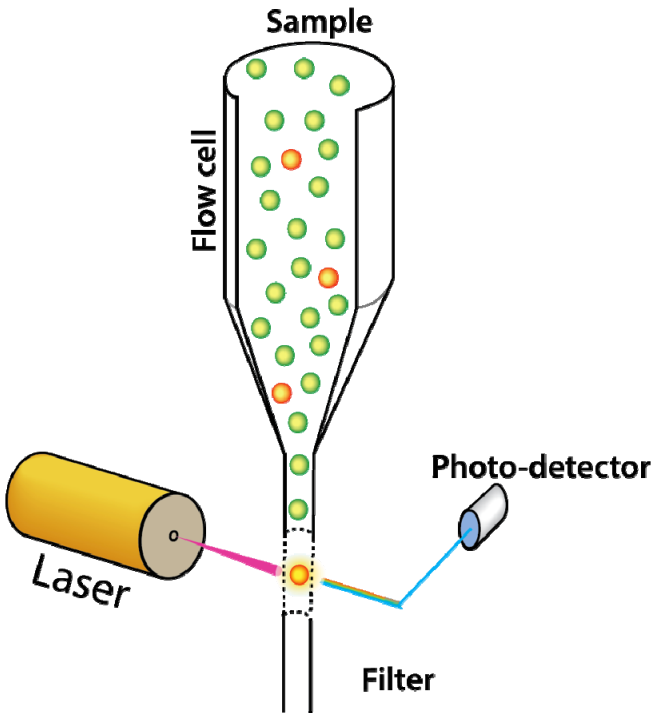
Pramod Murali, Igor Izyumin, Daniel Cohen,
Jun-Chau Chien, Ali M. Niknejad
and Bernhard Boser

University of California, Berkeley

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Introduction

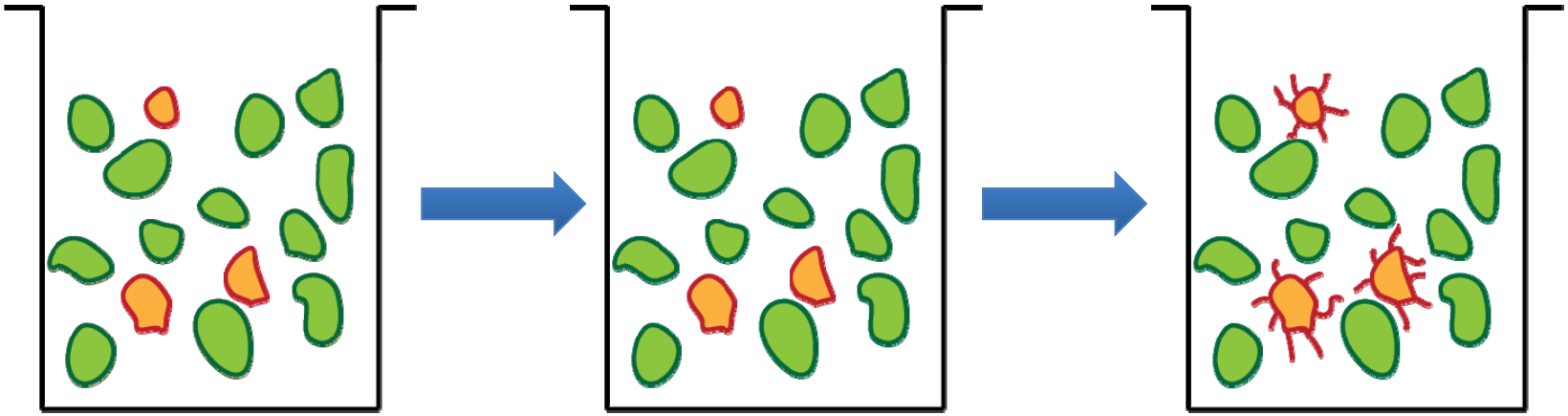
- Flow Cytometer
 - A diagnostic device that can to count and characterize specific cells in a sample.
- Applications
 - Infectious diseases and Cancer
 - Pathogen detection
 - Research



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Optical Flow Cytometry

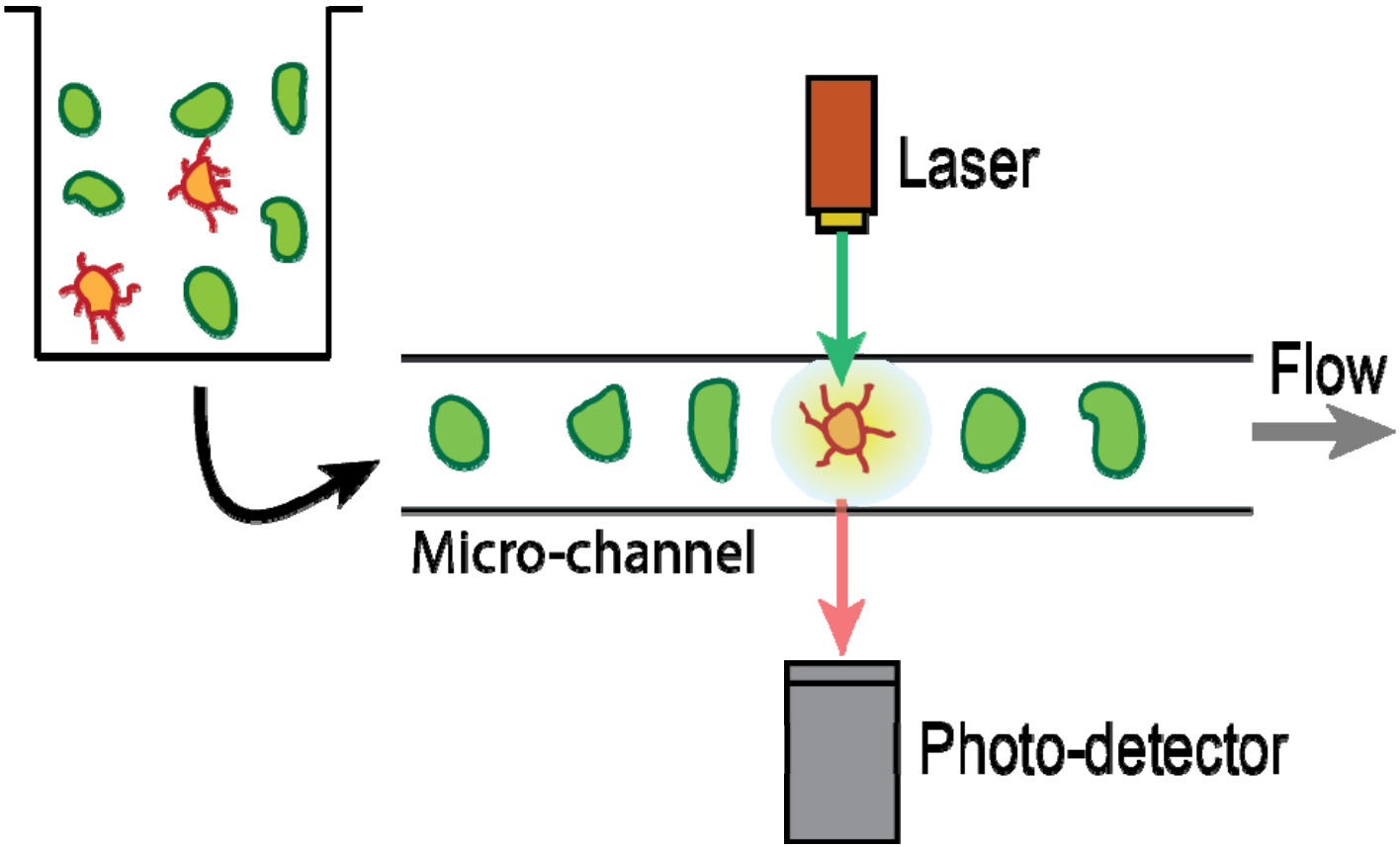
- Fluorescent Labels



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Optical Flow Cytometry

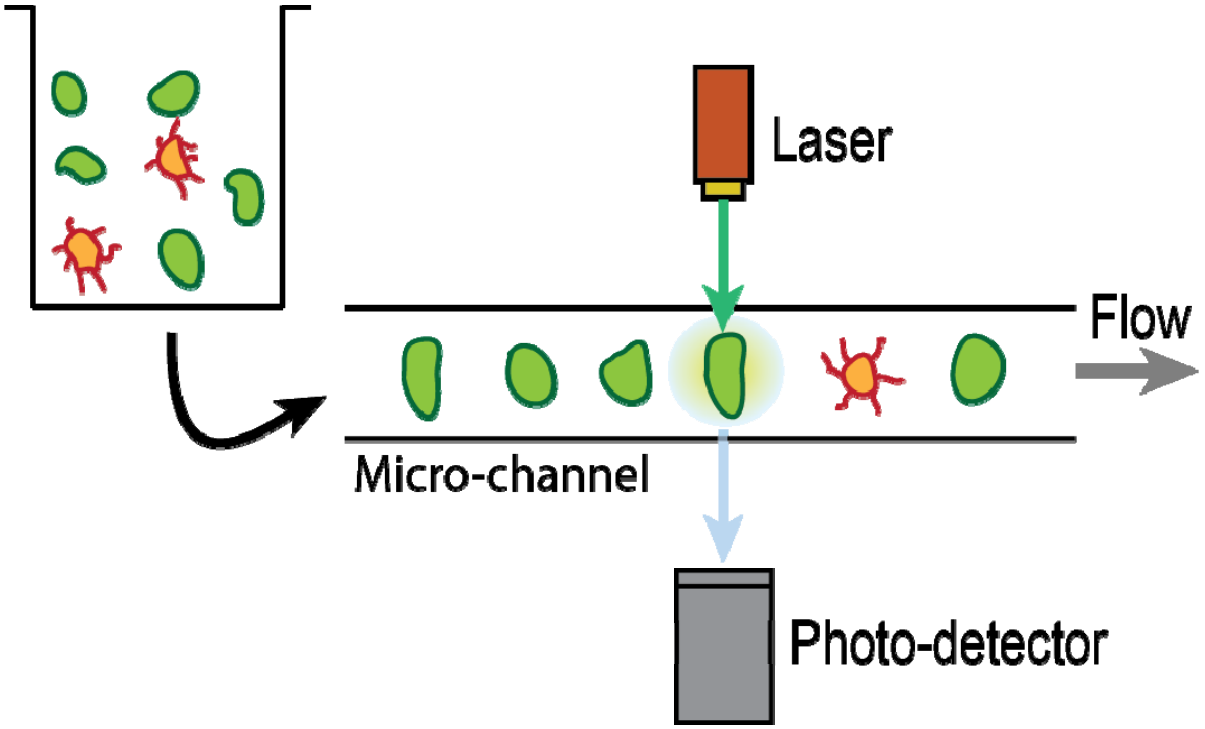
- Fluorescent Labels



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Optical Flow Cytometer

- Limitations

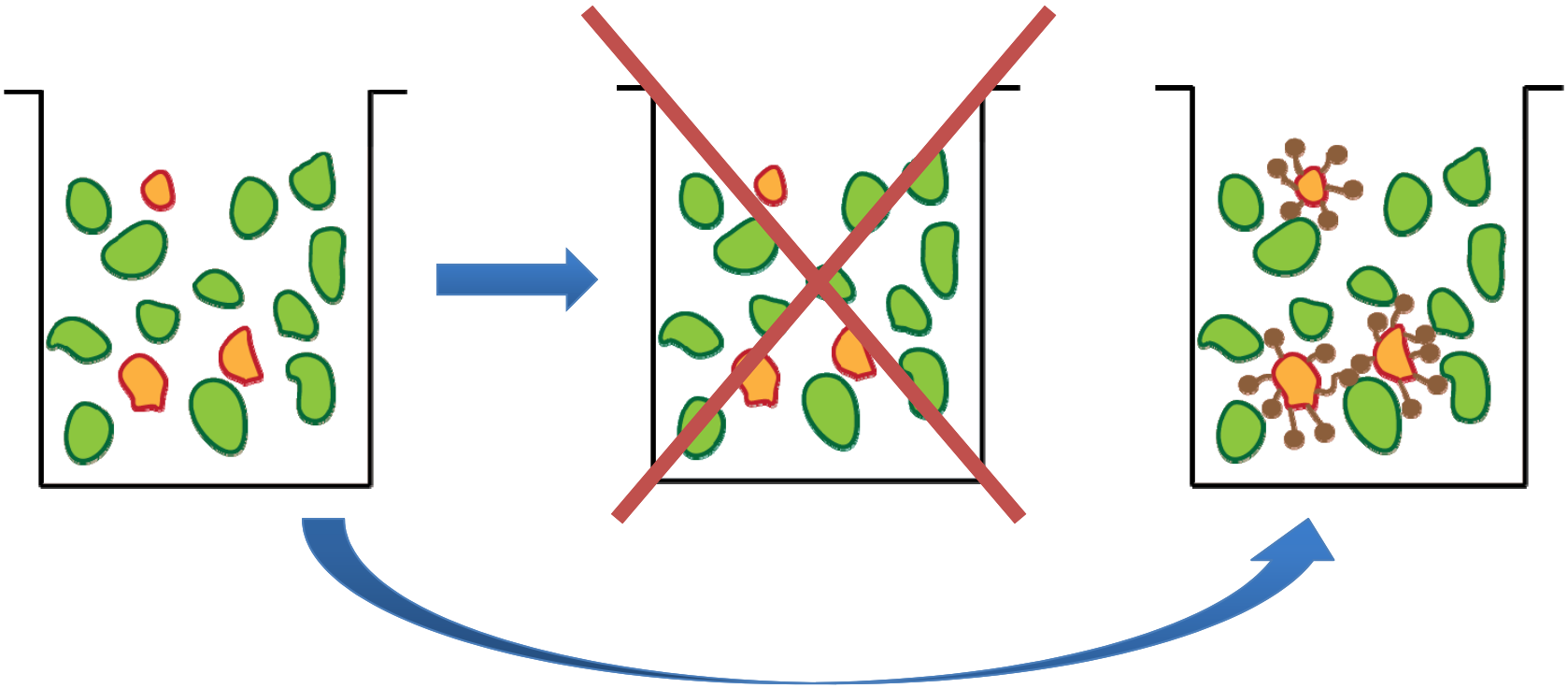


- Background of unlabeled cells
- Calibration
- Lab facilities

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Magnetic Flow Cytometry

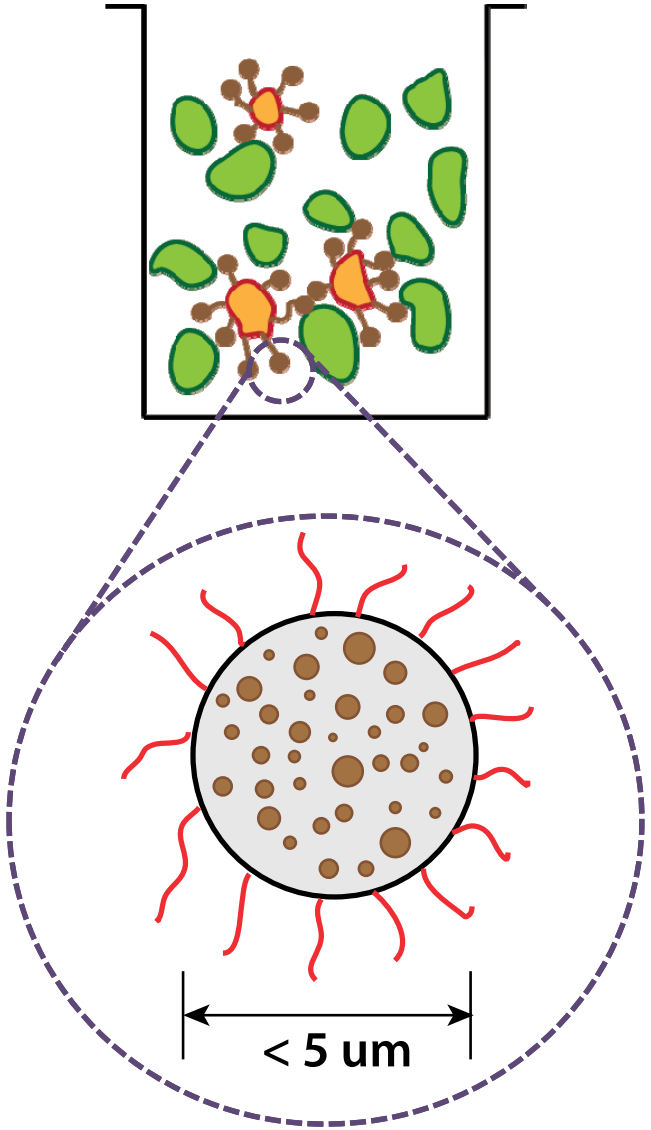
- Magnetic labels

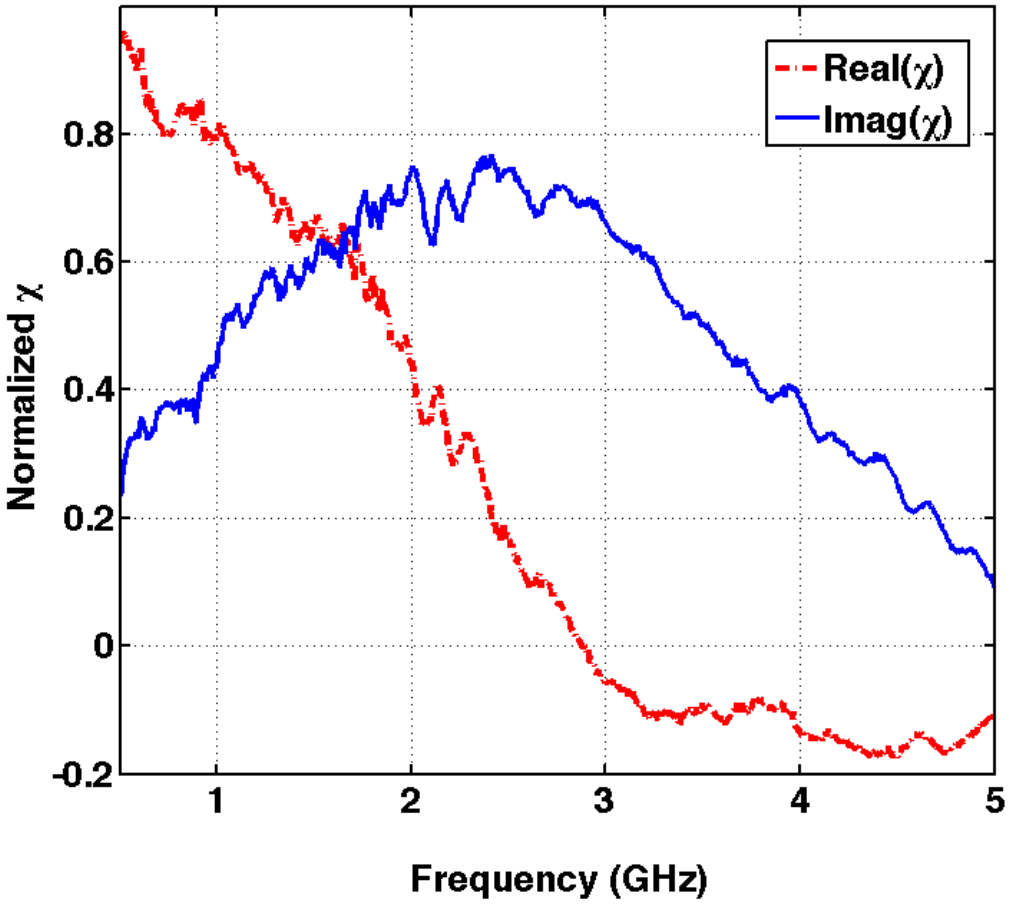


[Helou et. al. Lab-on-Chip 2013]

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Magnetic Labels

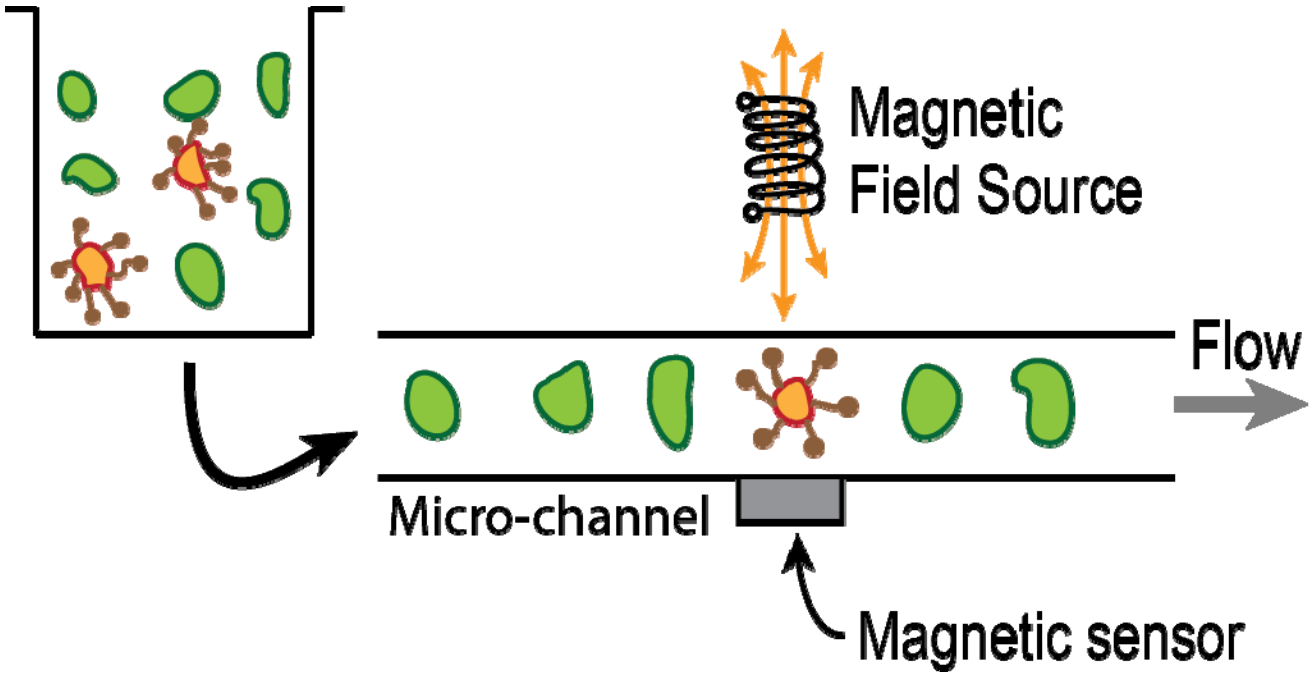




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Magnetic Flow Cytometer

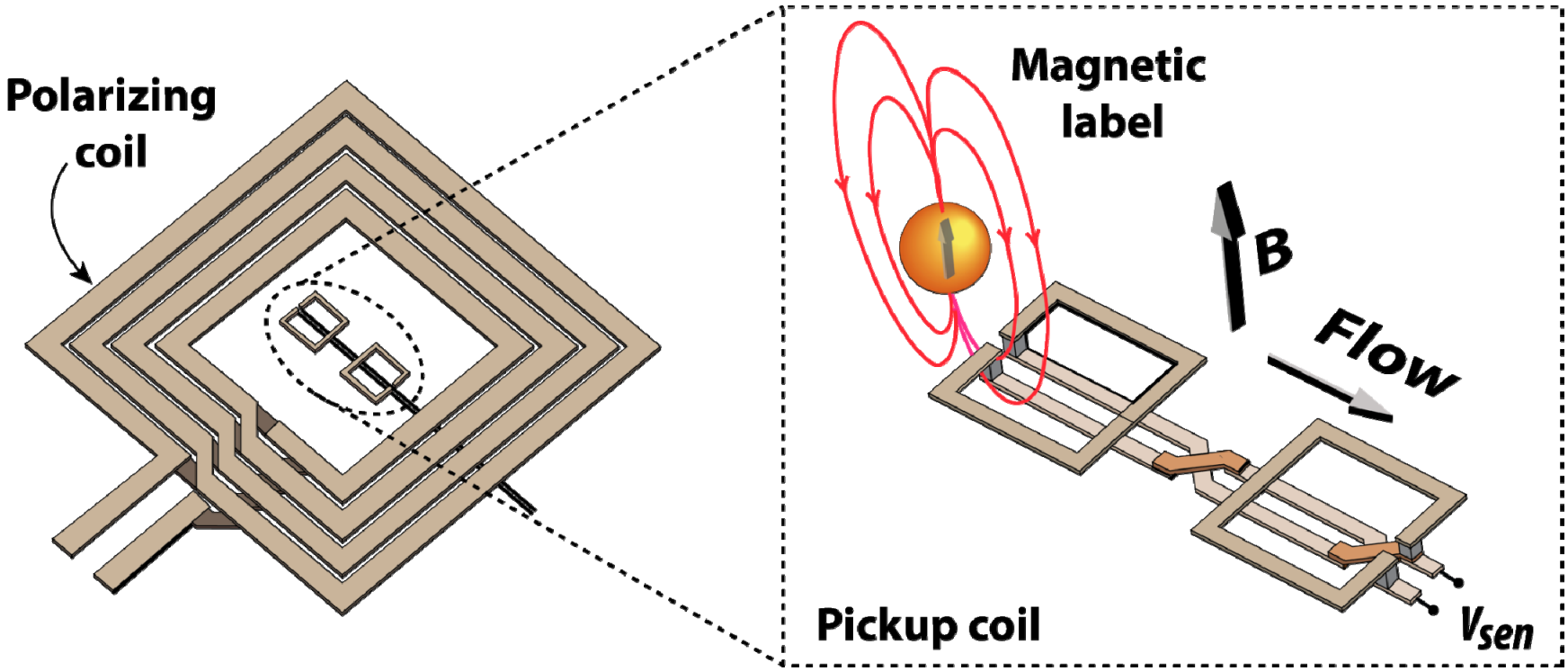
- Magnetic labels



- No background
- No calibration
- No lab facilities

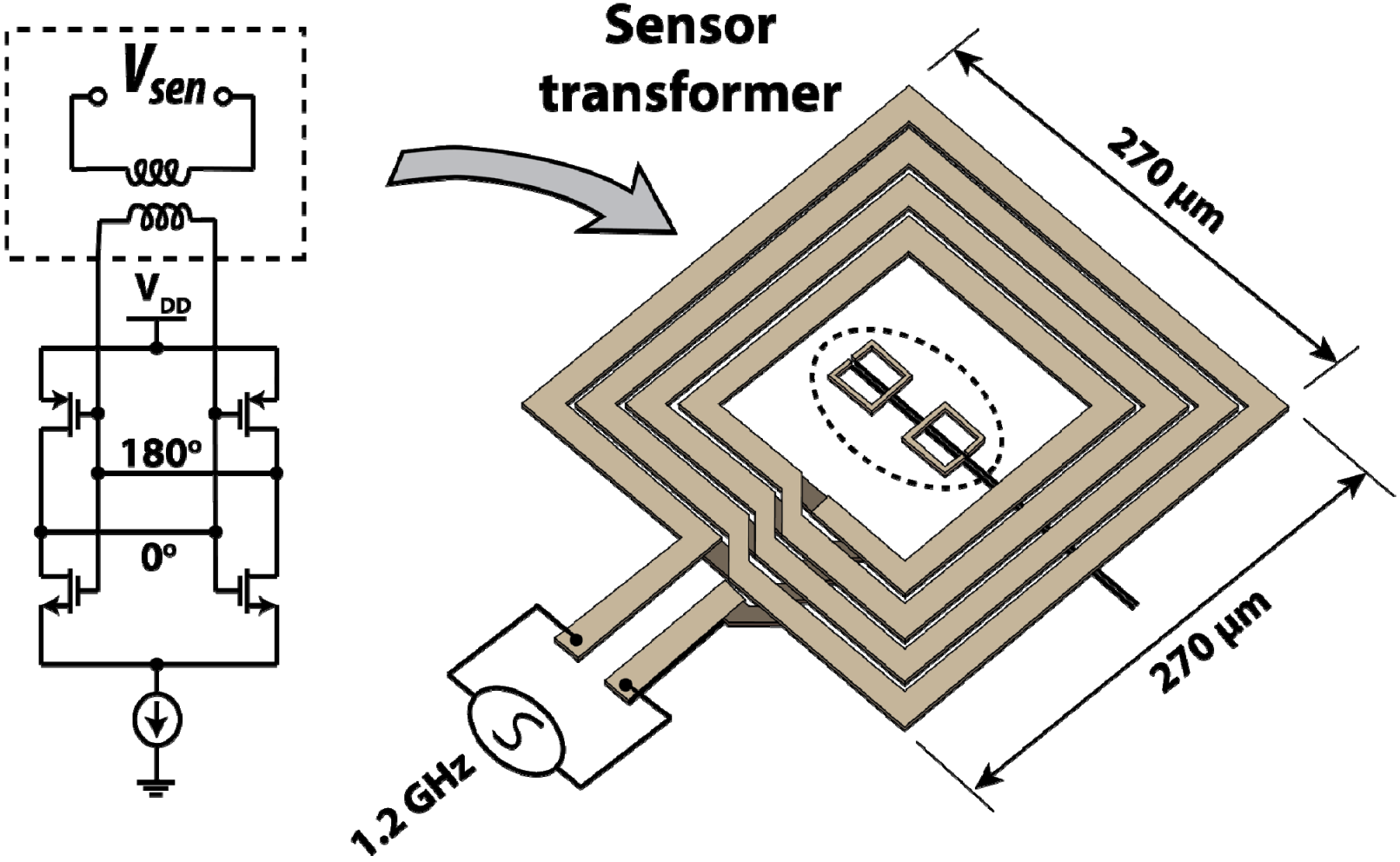
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Magnetic Sensor



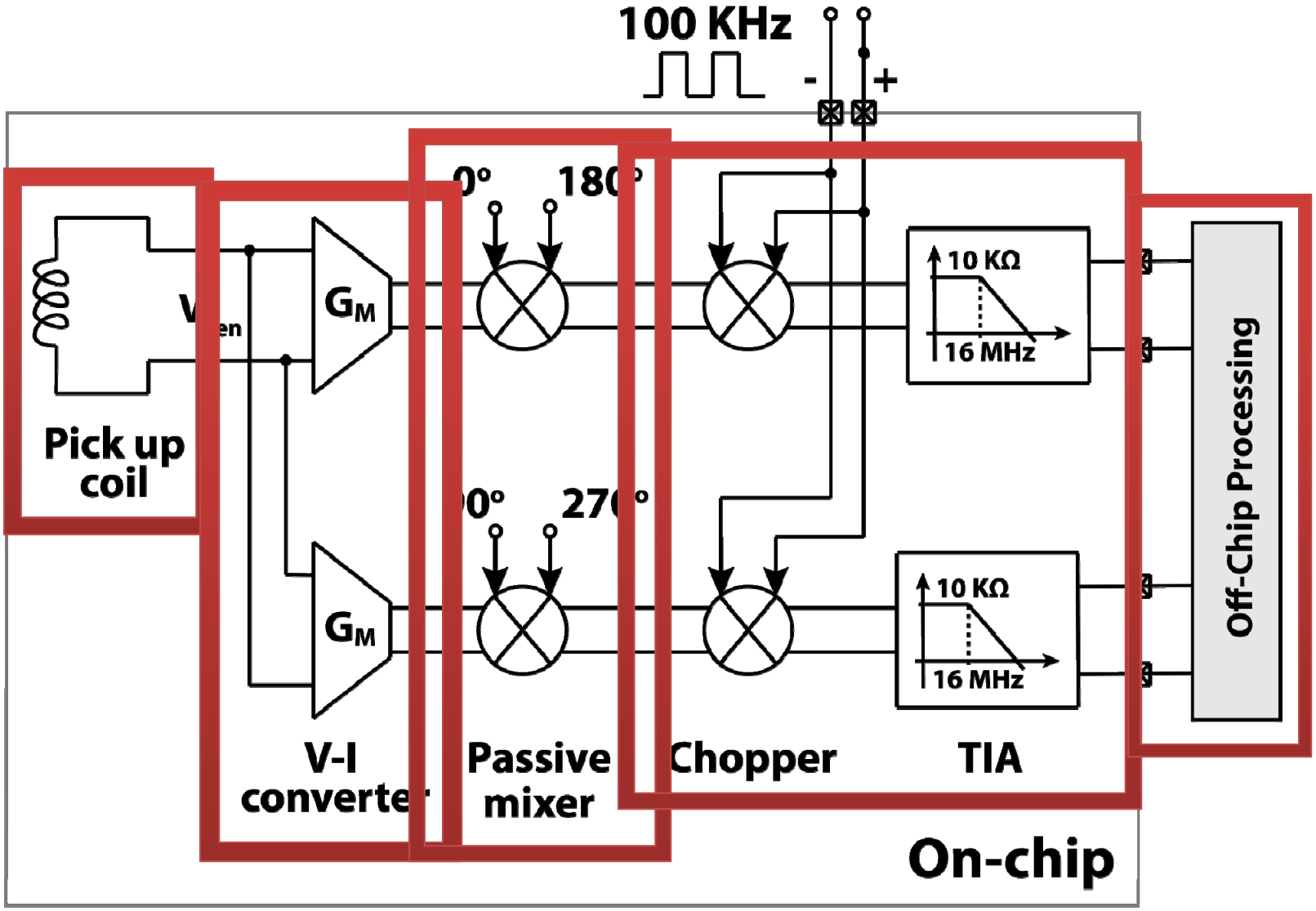
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Magnetic Sensor : Excitation



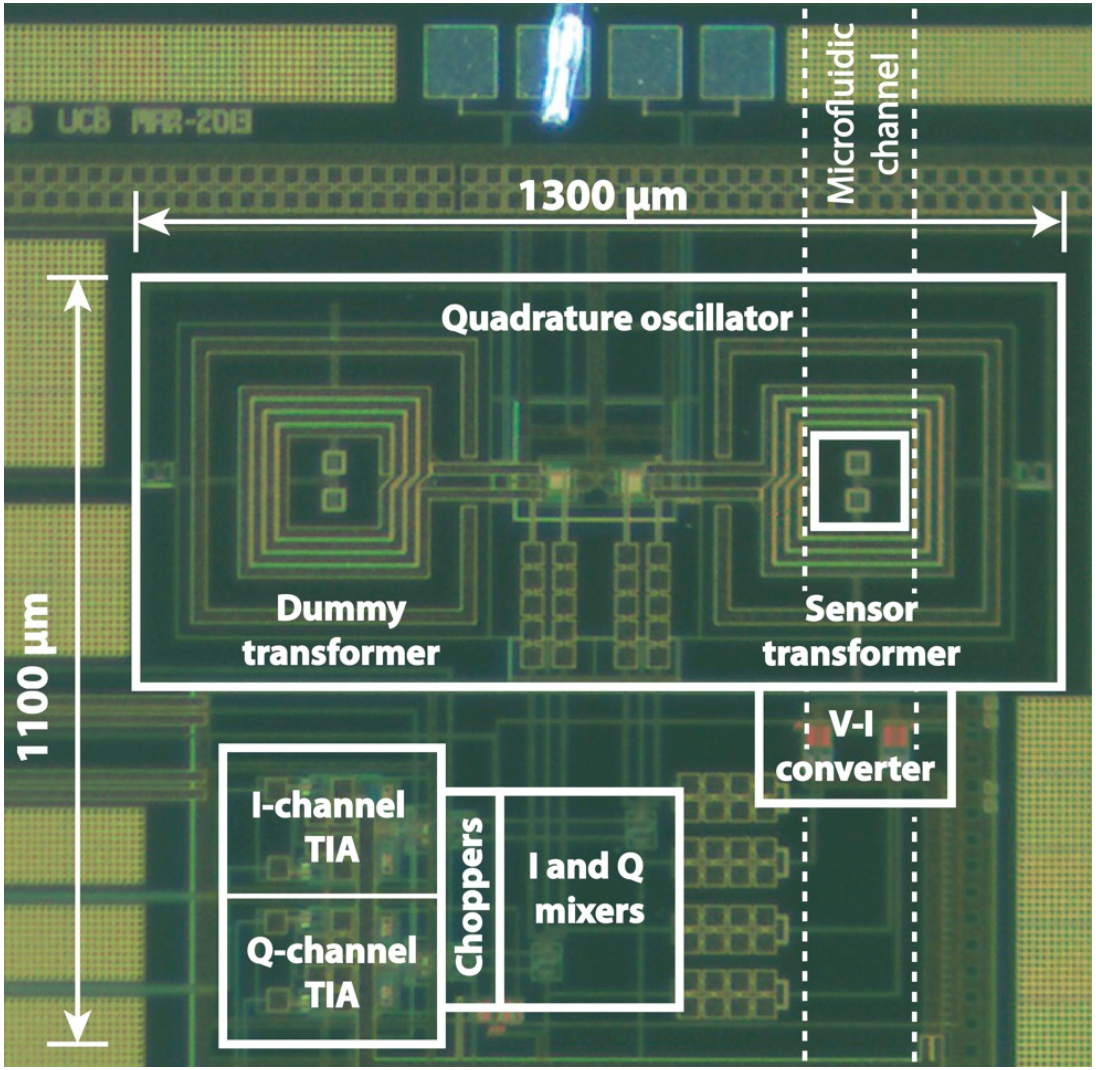
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Chip Architecture



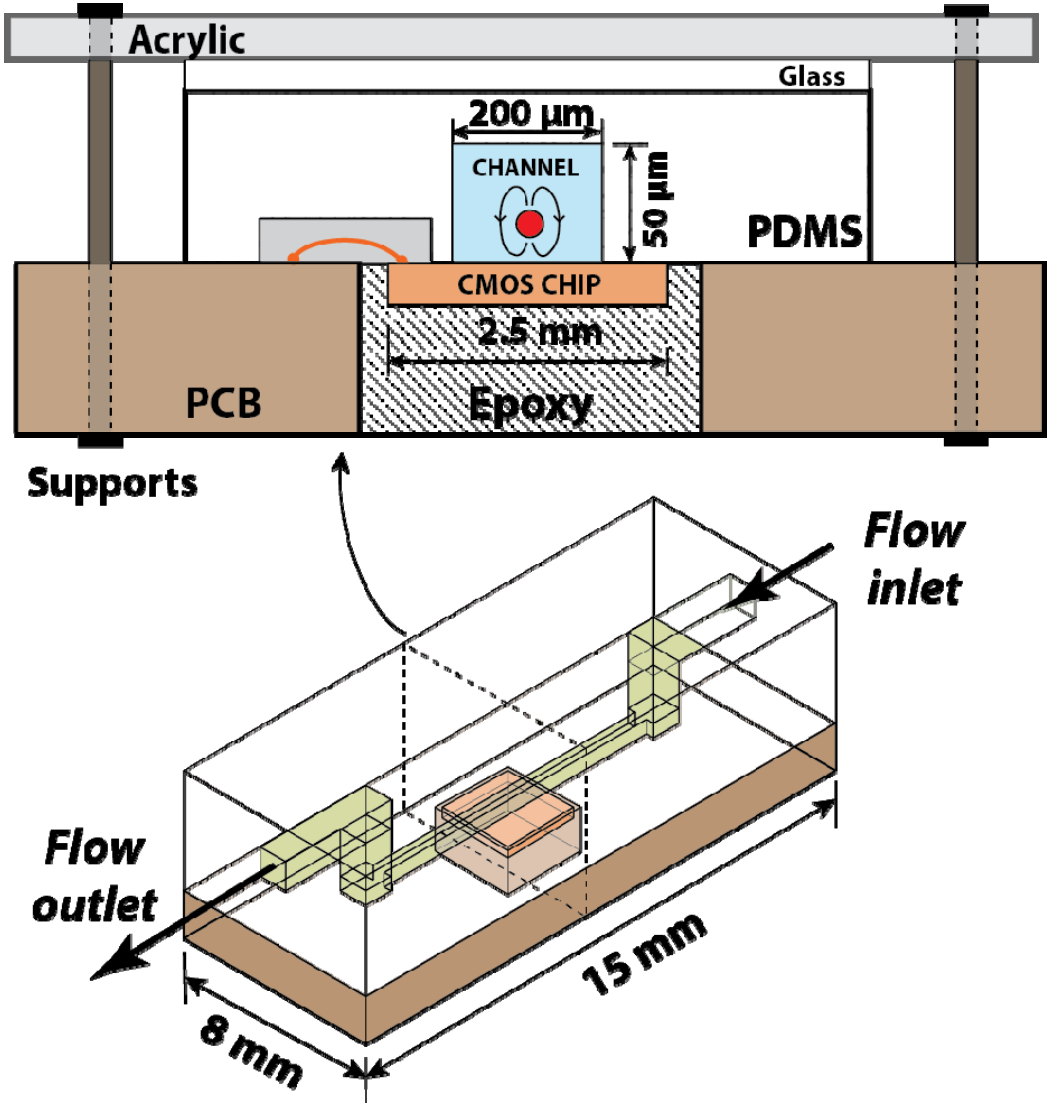
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Chip Photograph



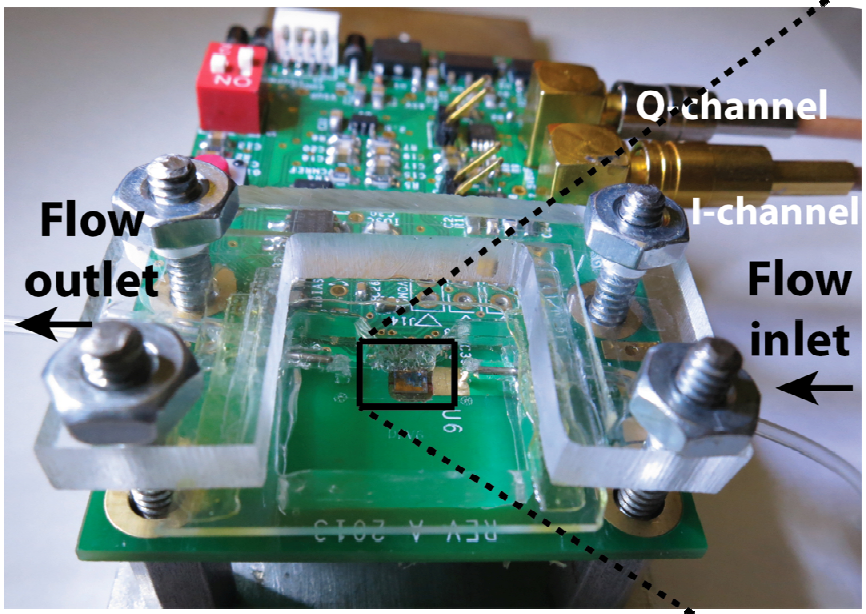
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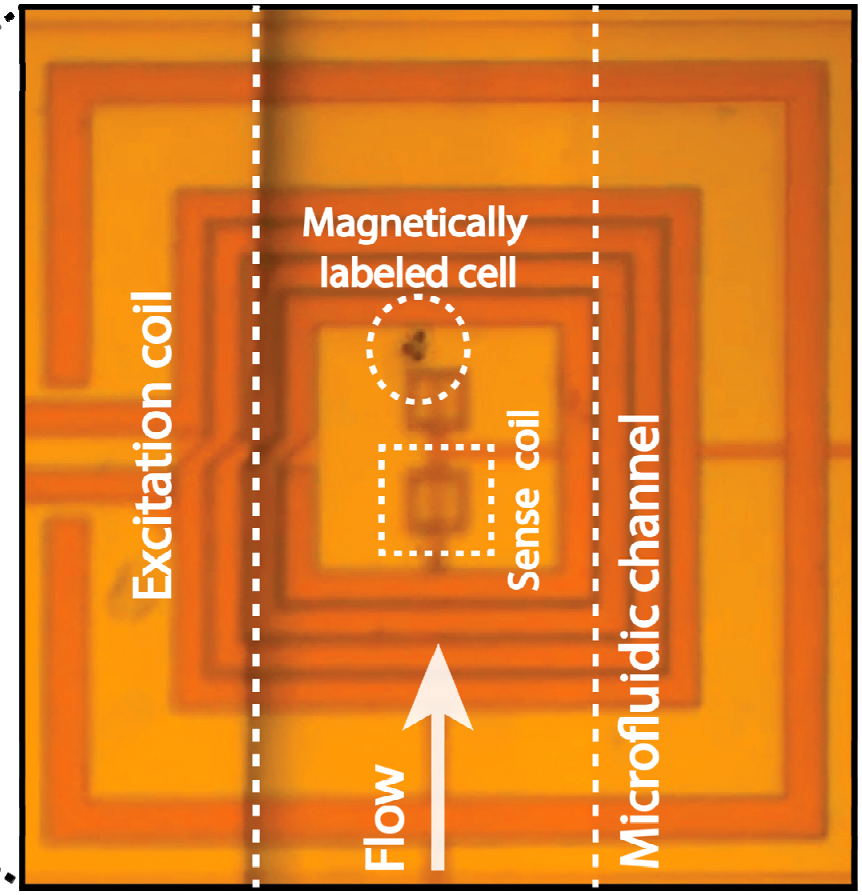
Microfluidic Integration



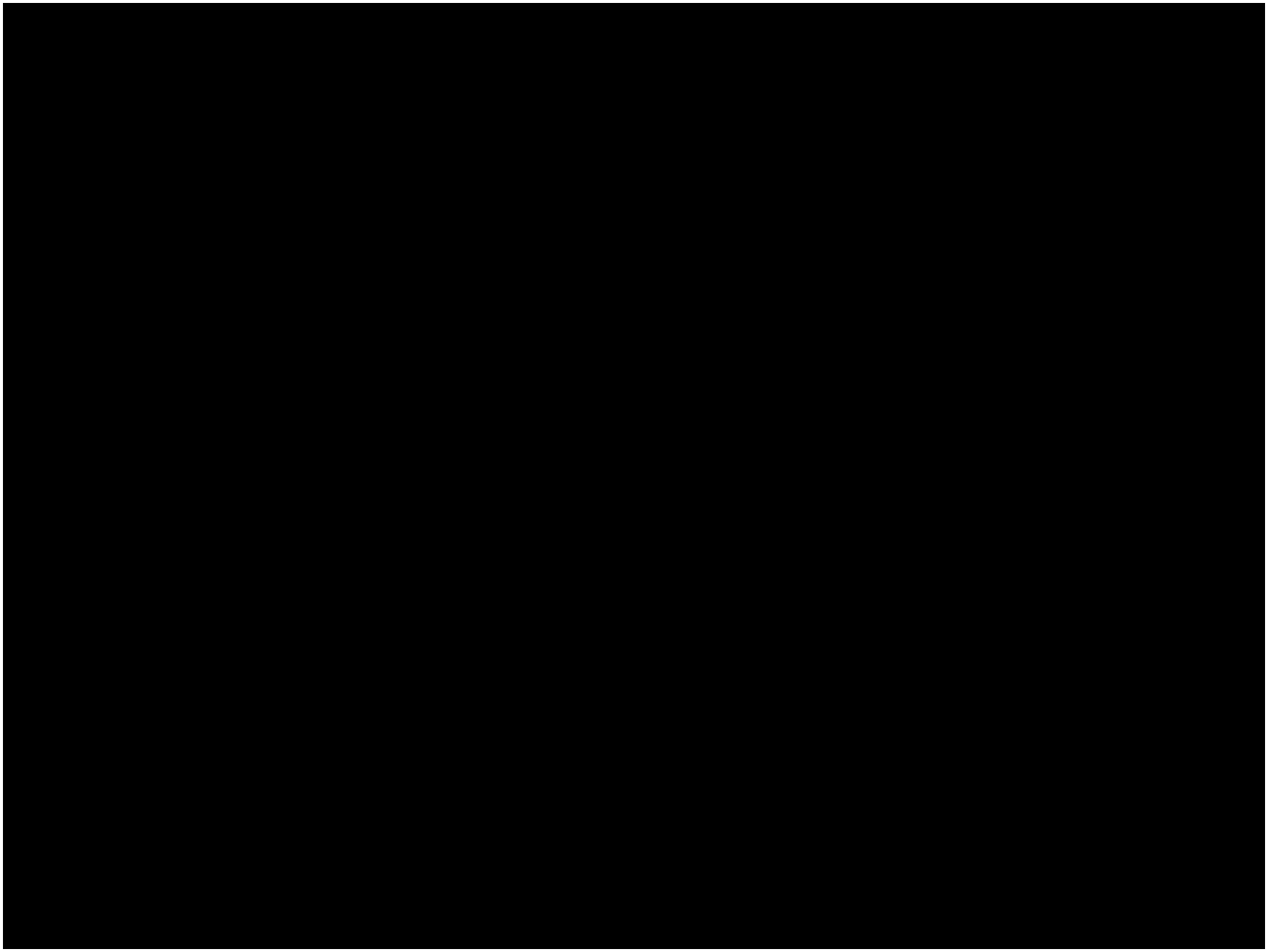
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Flow Cytometer Setup



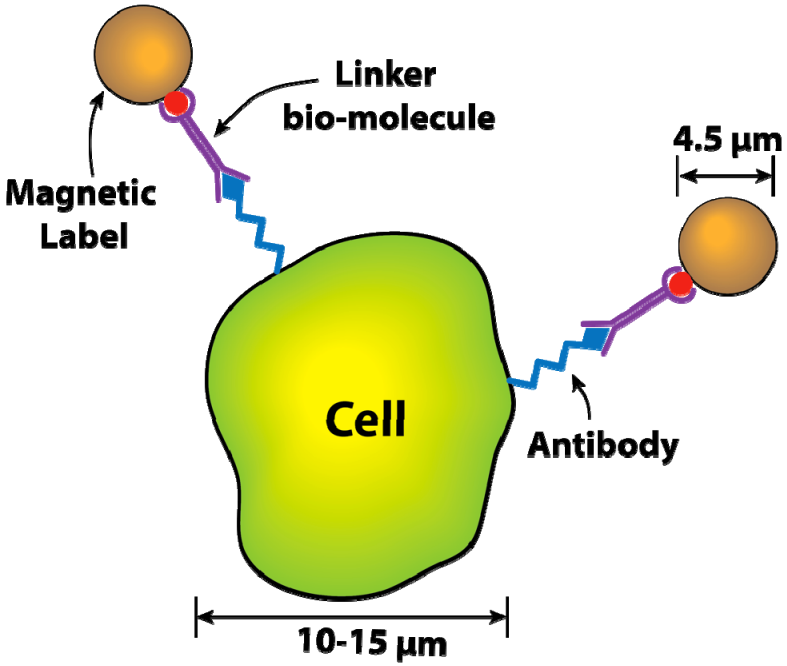


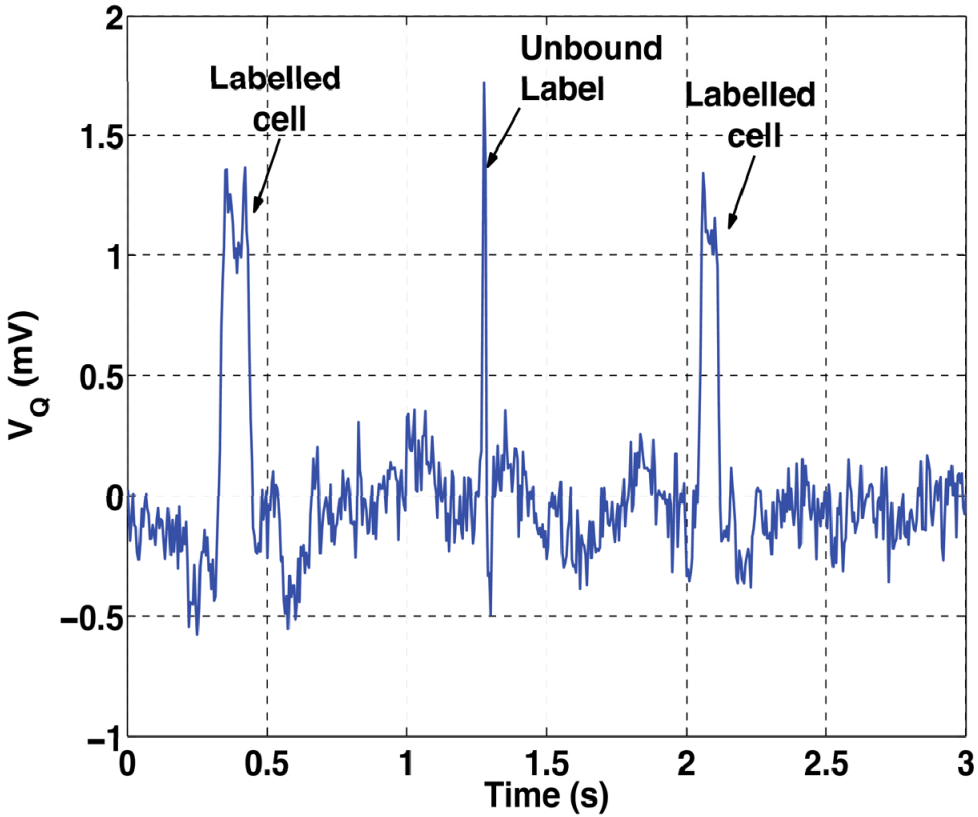
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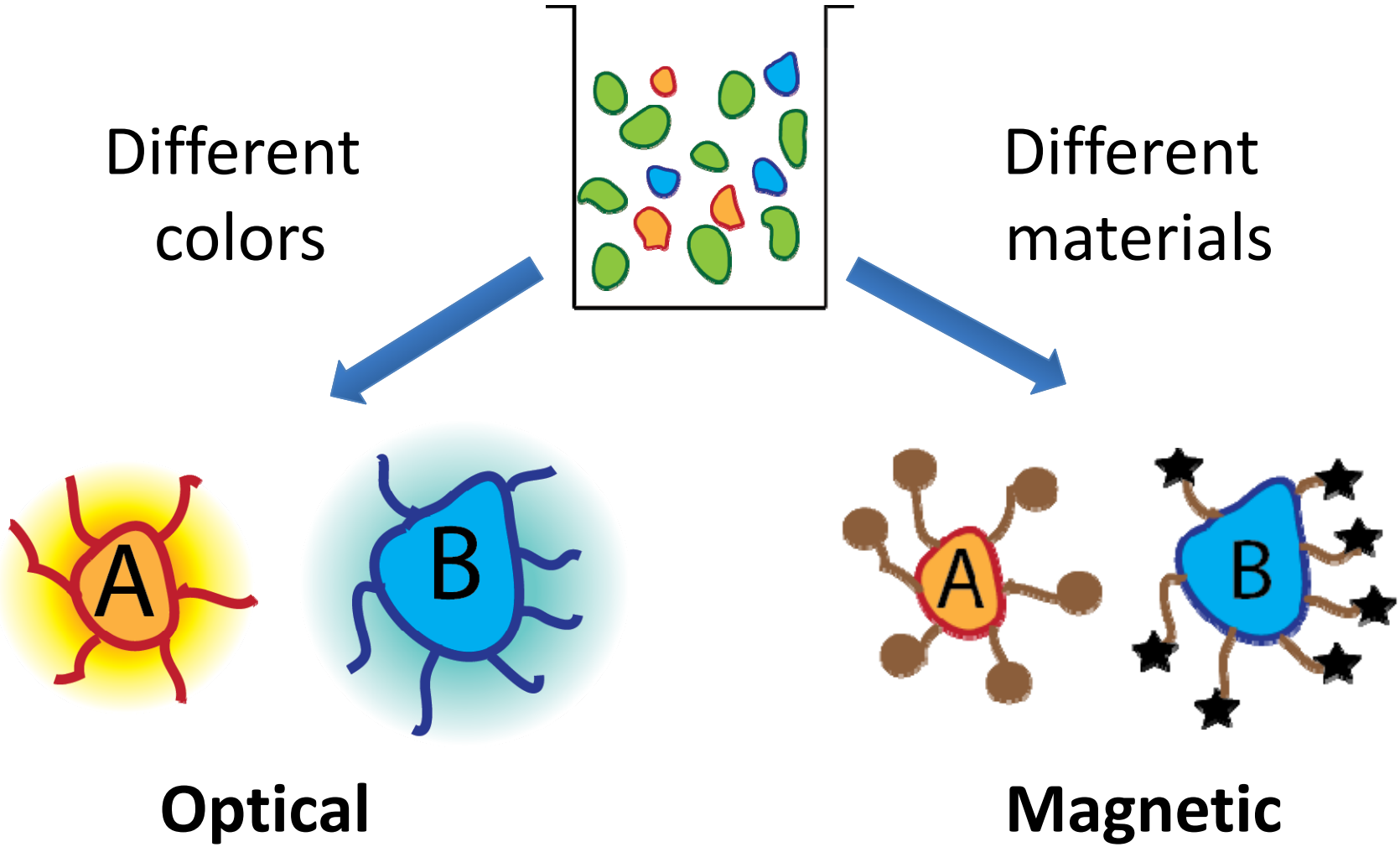
Cell Labeling and Detection





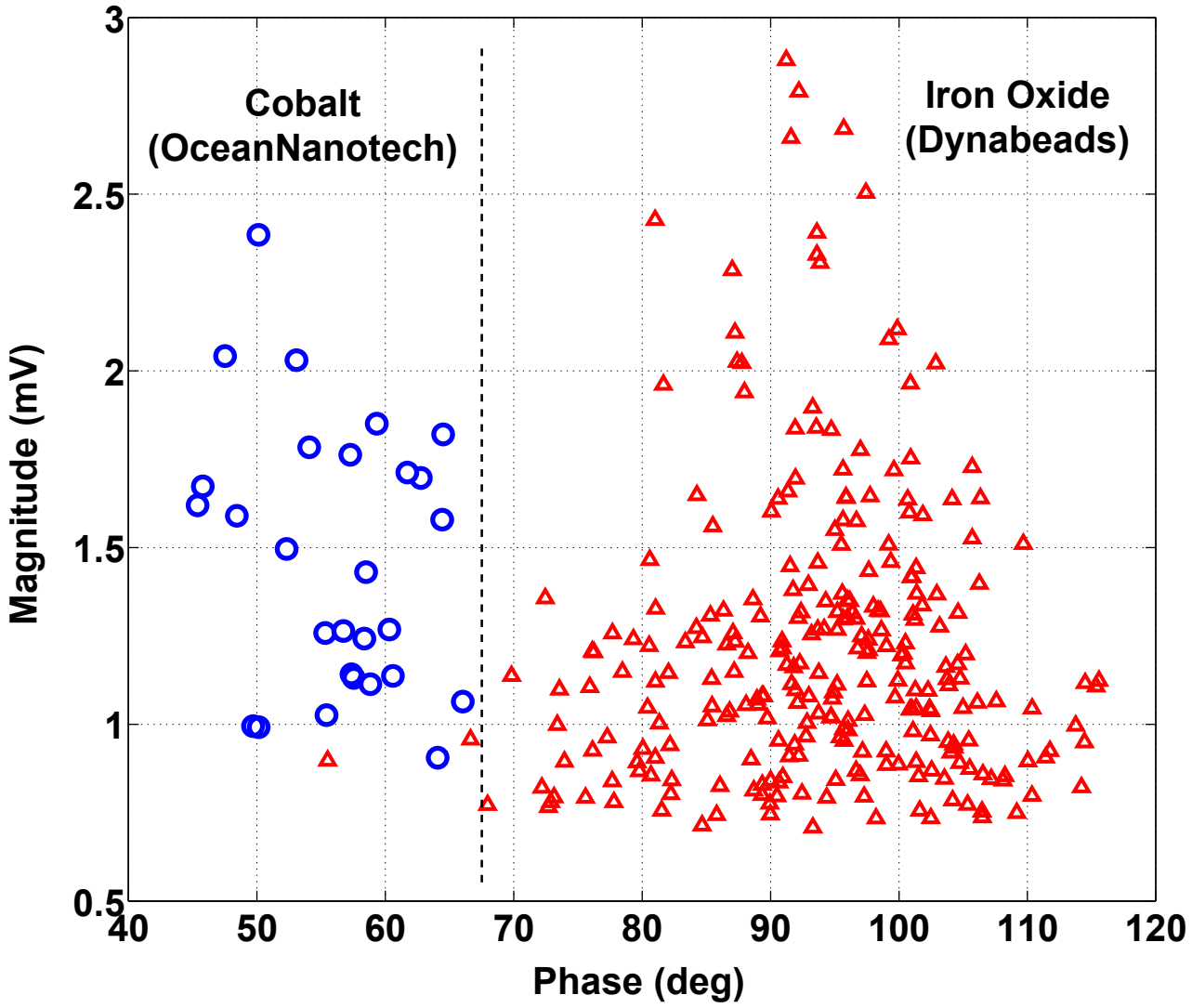
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Multiple Labels



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Multi-Label Classification



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Comparison Results

	ISSCC 2012 [1]	Trans. Medicine 2012 [2]	Lab-on-Chip 2013 [3]	ISSCC 2013 [4]	**This work**
Sensor	Electrode pair	μHall Detector	GMR	LC Tank	**Spiral Transformer**
Sensor integration	Off-chip	N/A	N/A	On-chip	**On-chip**
Application	Cell counter	Flow cytometry	Flow cytometry	Immunoassay	**Flow cytometry**
External components	None	0.5 T Magnet	0.2 T Magnet	None	**None**
Labels	None	$MnFe_2O_4$	FeO_x	FeO_x	**FeO_x and Co**
Separate Label Classes	0	3	1	2	**2**
Detection Time	50 ms	0.02 ms	40 ms	120 s	**20 ms**

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Thank You !

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A 60nV/√Hz 15-Channel Digital Active Electrode System for Portable Biopotential Signal Acquisition

Jiawei Xu[1,3], B. Büsze[1], H.Kim[2],

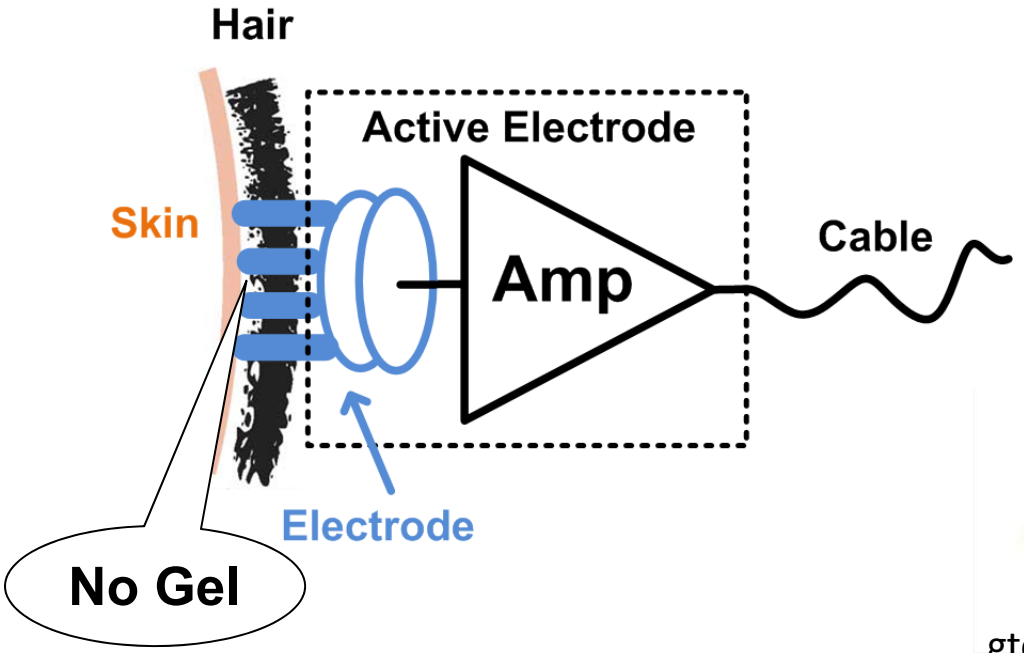
K.A.A. Makinwa[3], C. Van Hoof[2], R. F. Yazicioglu[1,2]

[1] IMEC-Holst Centre [2] IMEC

[3] Delft University of Technology

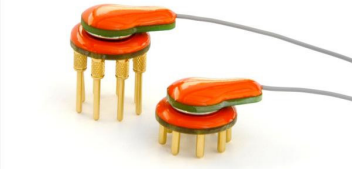
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Active Electrodes (AE) for EEG Recording





gtec- g.SCARBEO



gtec- g.SAHARAsys



imec- EEG headset

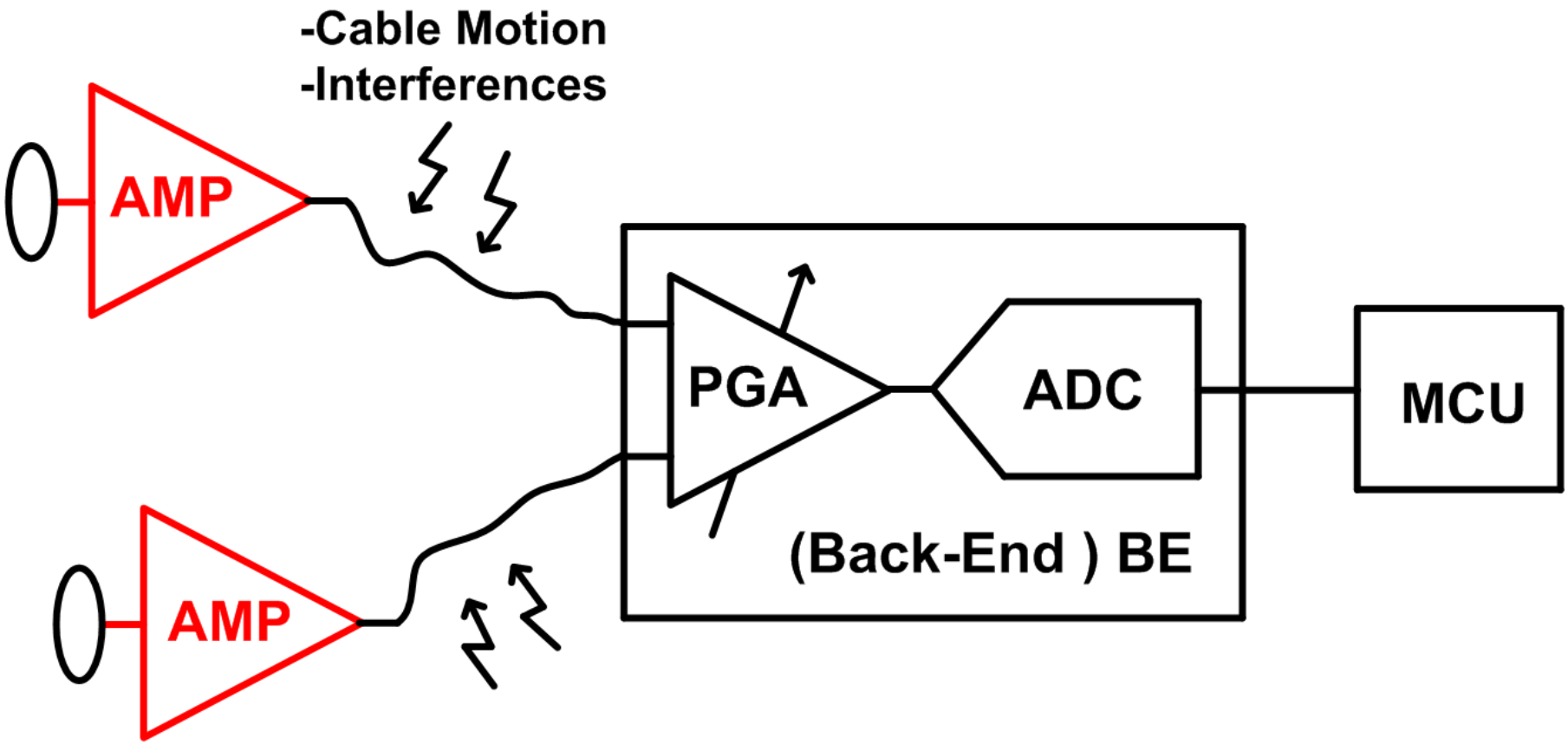
Active Electrode: co-integration of Amplifier and Electrode

- Amplifier: improved robustness to interference and cable motion
- Dry electrode: fast set-up, user comfort, long-term monitoring

Suitable for portable and wearable EEG and ECG measurement

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Existing “Analog” Active-Electrode System



Power hungry analog buffers

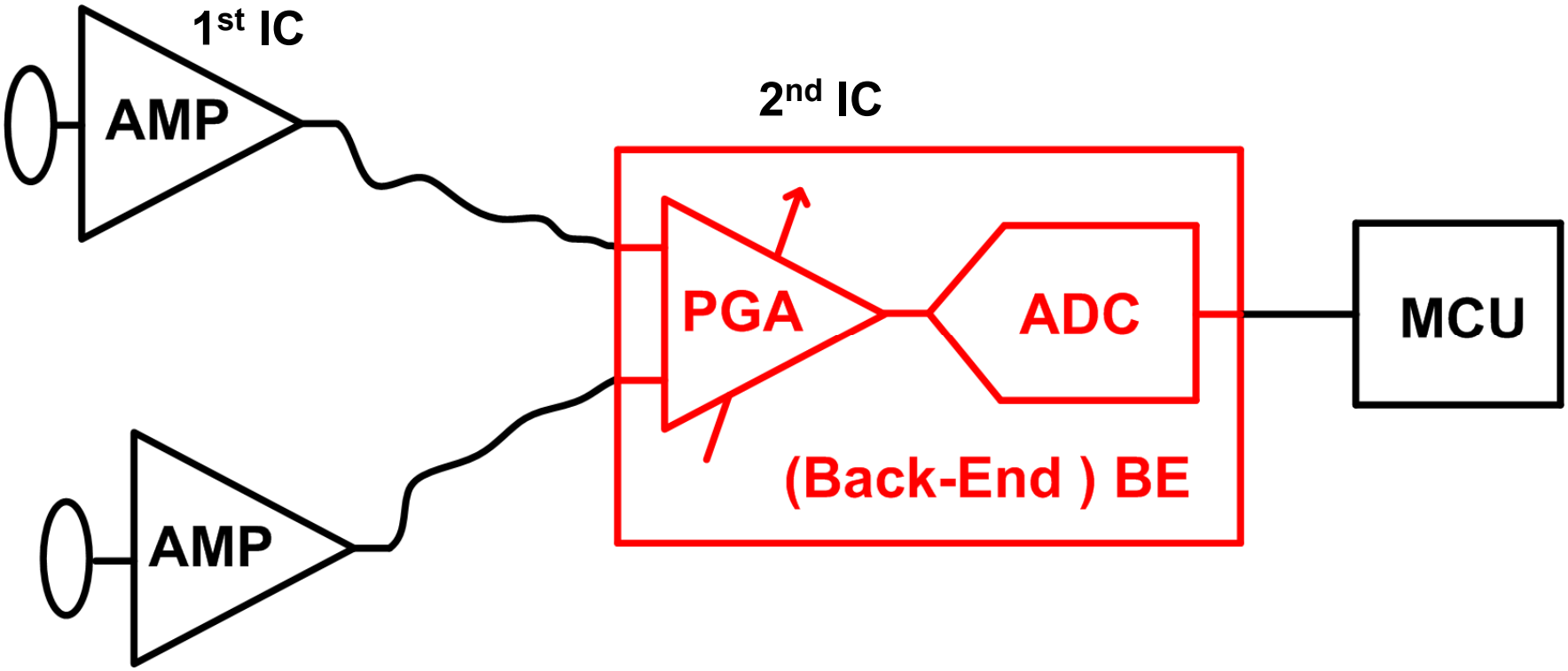
Back-End (BE) ASIC: system complexity and cost

Significant number of cables

AE mismatch: limited CMRR

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Existing “Analog” Active-Electrode System



Power hungry analog buffers

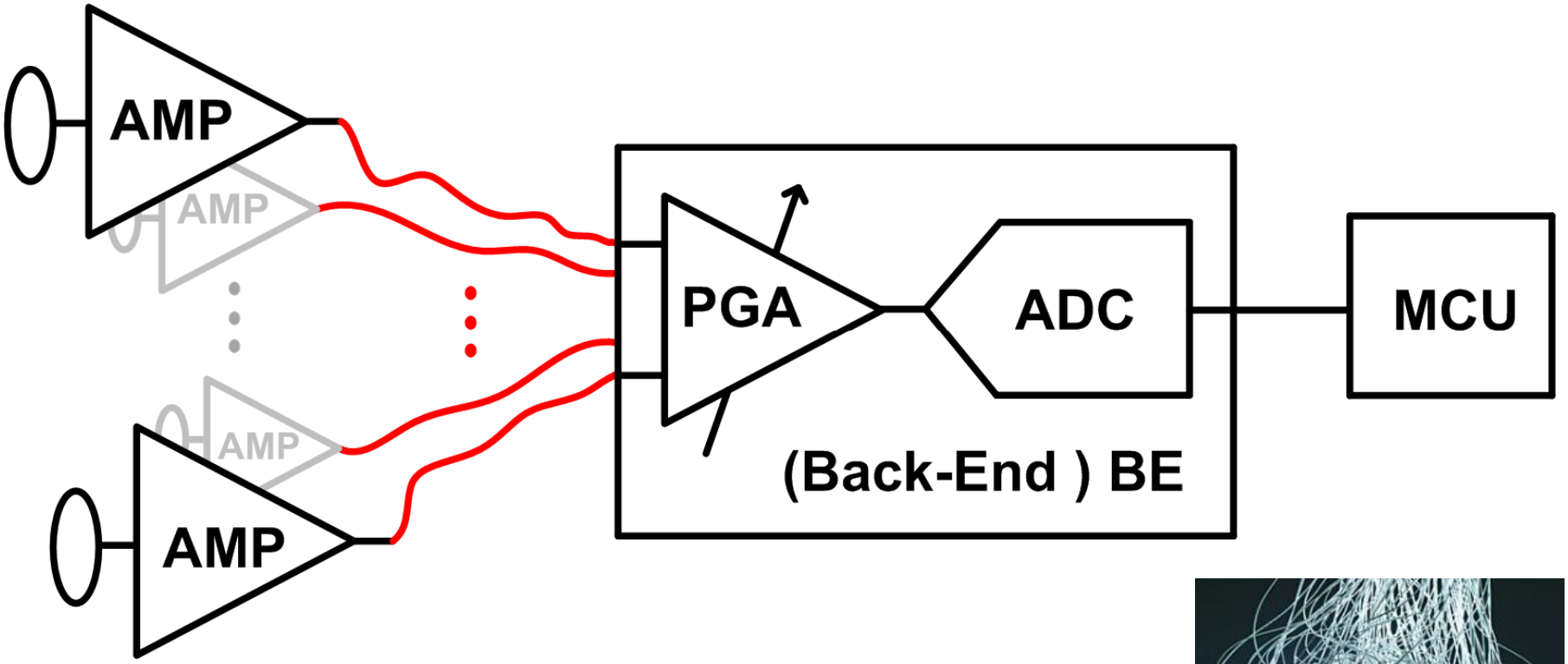
Two-chip solution: system complexity and cost

Significant number of cables

AE mismatch: limited CMRR

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Existing “Analog” Active-Electrode System





Power hungry analog buffers

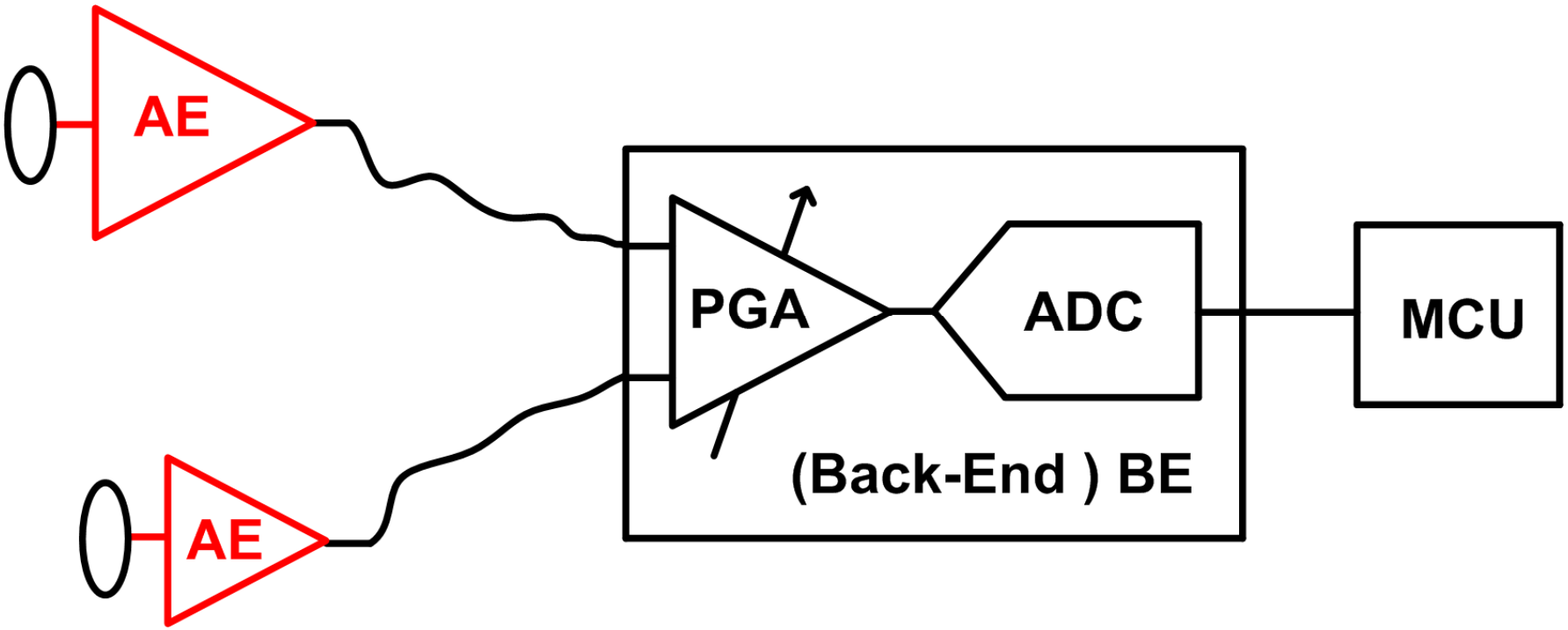
Back-End (BE) ASIC: system complexity and cost

Significant numbers of cables: volume and weight

AE mismatch: limited CMRR

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Existing “Analog” Active-Electrode System



Power hungry analog buffers

Back-End (BE) ASIC: system complexity and cost

Significant number of cables

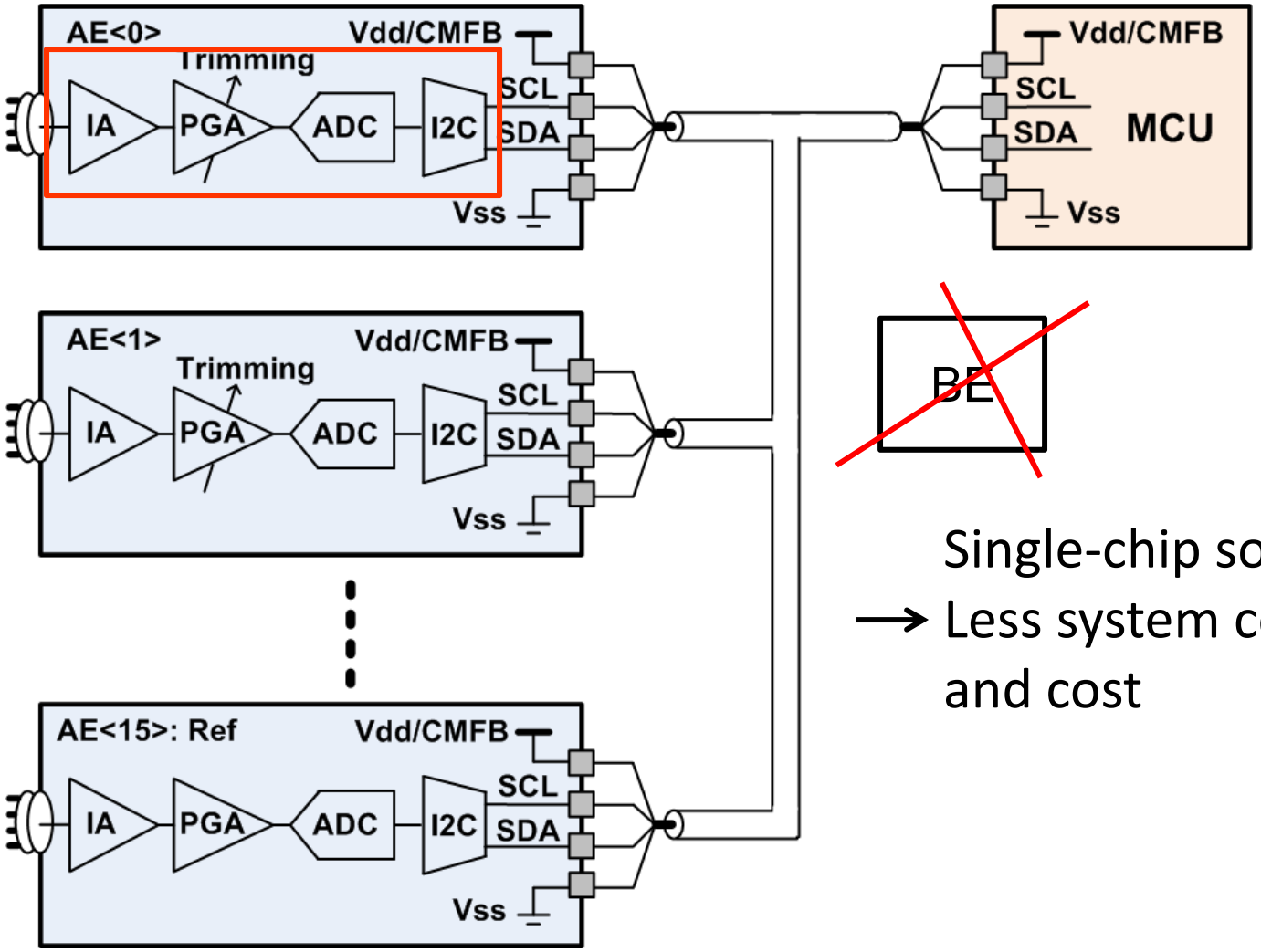
Components mismatch: limited system CMRR

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Digital Active Electrode (DAE) System

Amplifiers, ADC, and digital interface are fully integrated

→ Digital outputs are more robust to cable motion artifact

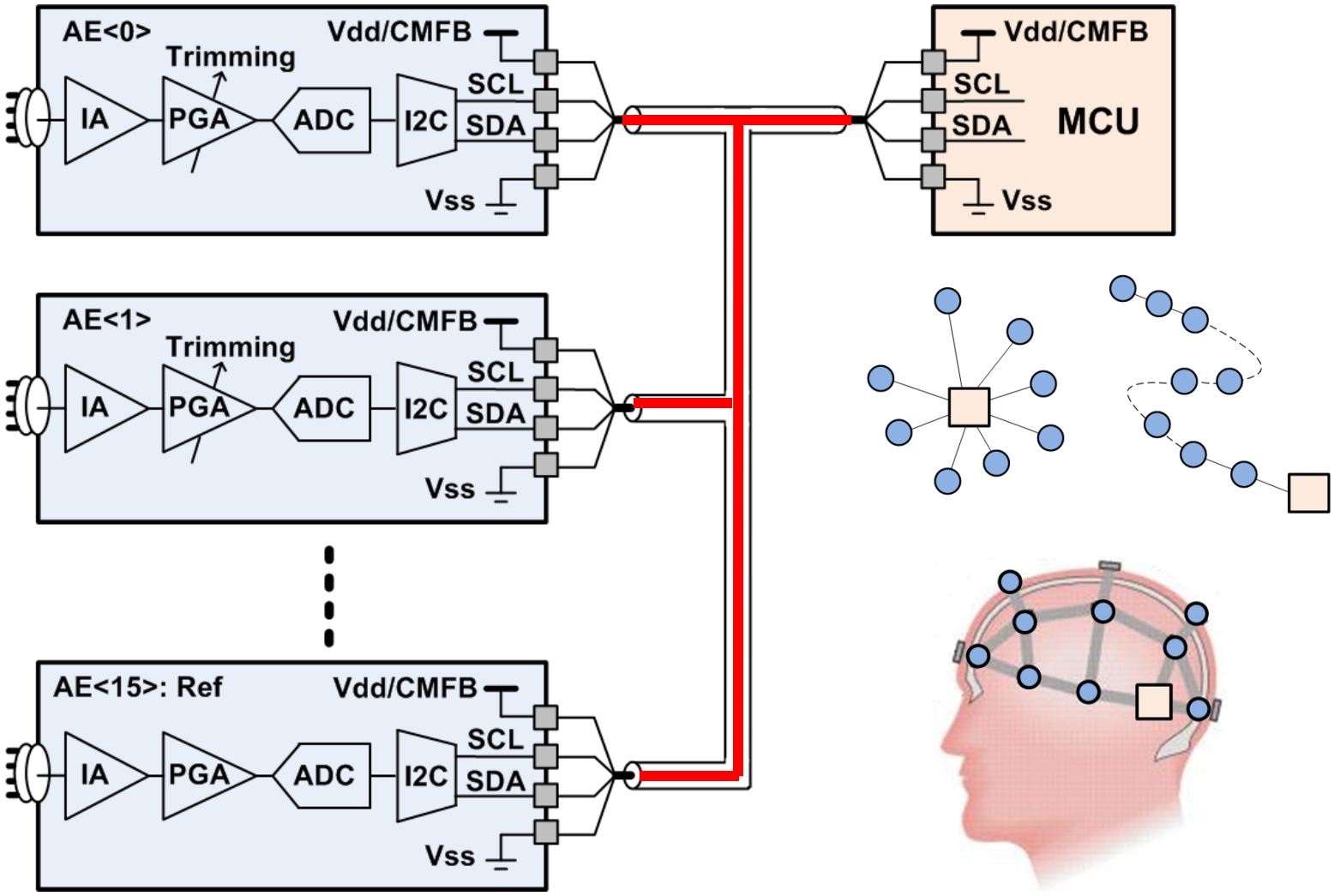


Single-chip solution

→ Less system complexity and cost

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Digital Active Electrode (DAE) System

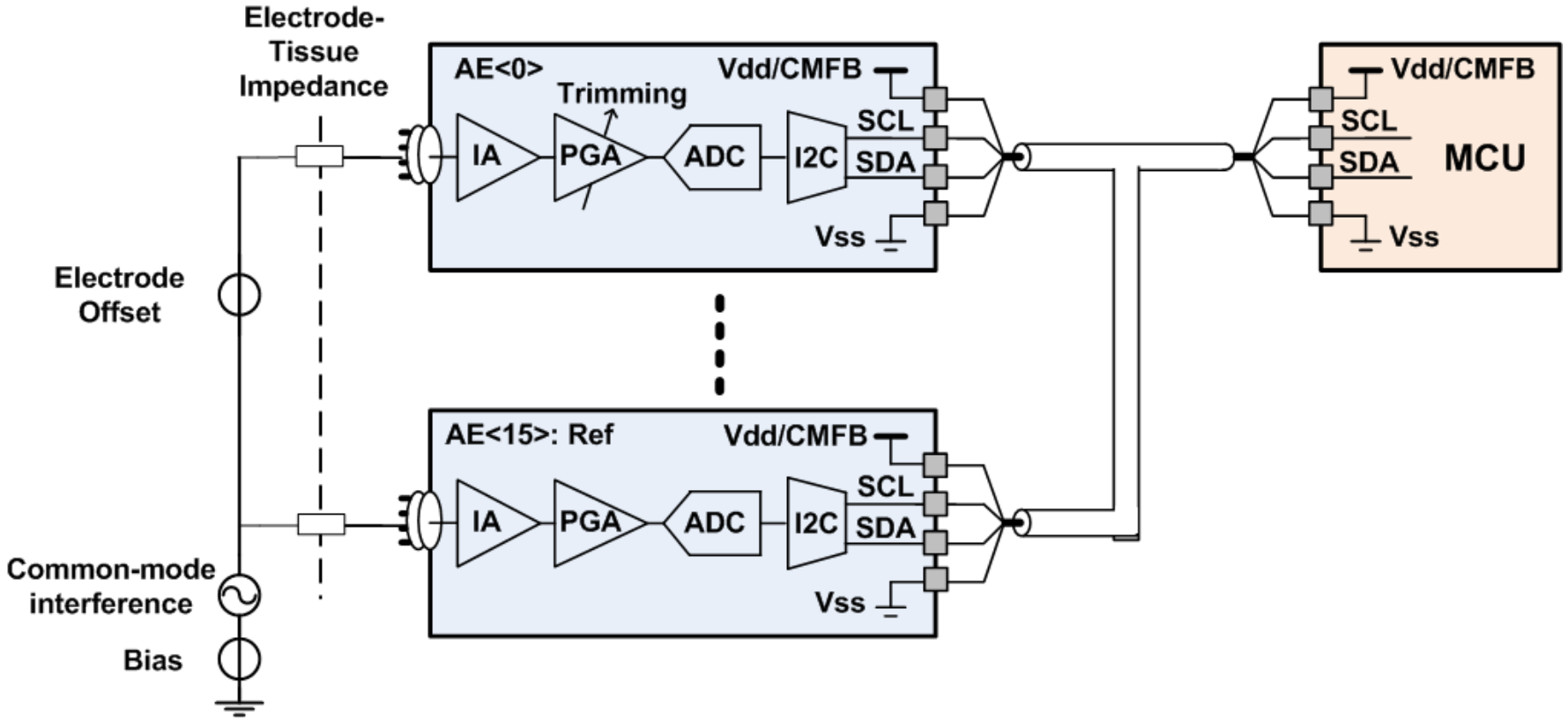


4-wire I2C bus: compatible to MCU and medical grade cable

Star or series connection for variable devices: headset, cap, band...

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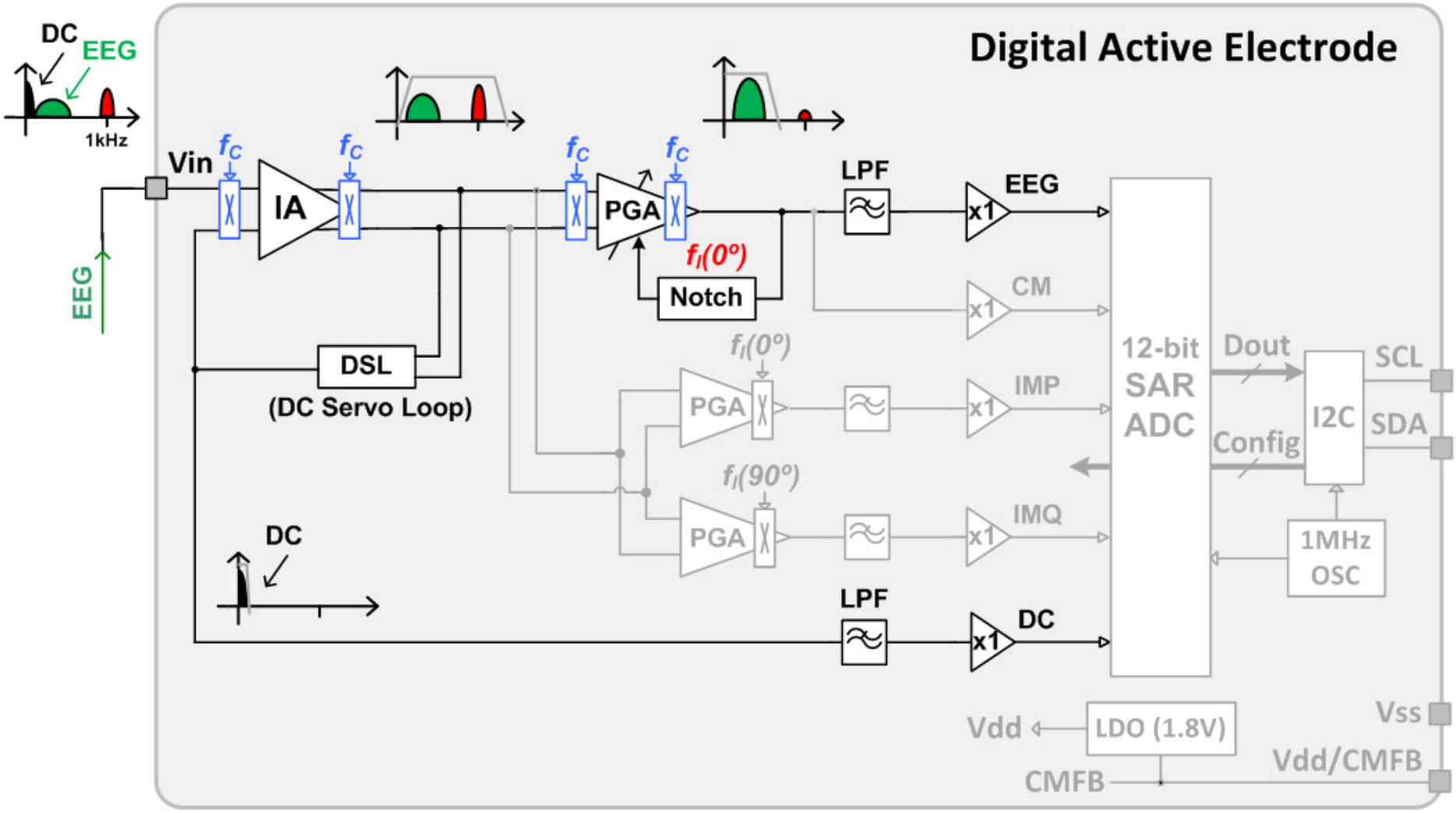
Design Challenges in IC and System



- Achieve <100 nV/sqrt(Hz) input noise over ±300 mV electrode offset, >100 MΩ input impedance of IA for dry electrode
- Compensate >10 mV common-mode interference for single-ended amplifier with high gain (700-1400)
- >80db CMRR without adding significant system complexity and power

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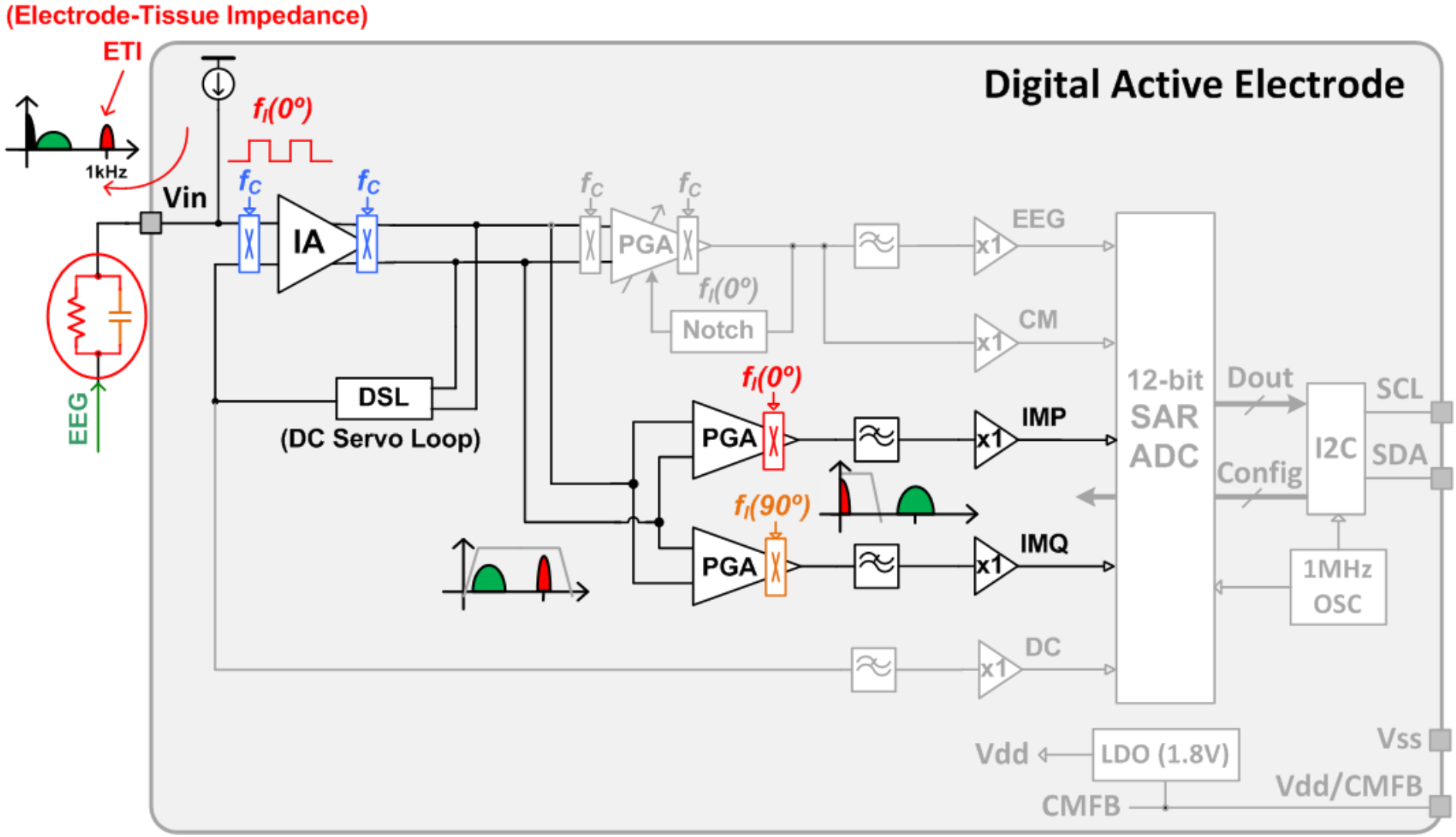
EEG and DC Measurement



- EEG: AC-coupled, gain 140\700\1400, BW: 0.5-100 Hz
- DC and infra-low-frequency signal: unit-gain, BW: DC-0.5 Hz

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Electrode-Tissue Impedance (ETI)

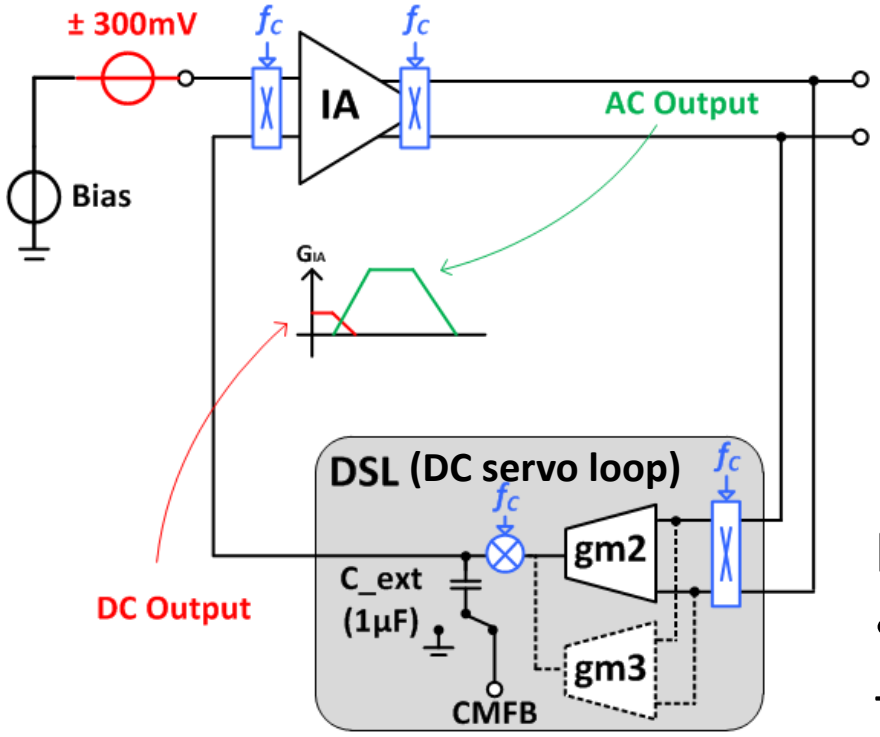


Simultaneous EEG/ETI recording, current injection: 10 nA-2 µA @1 kHz

Resistive and Capacitive ETI measurement up to 400 kΩ@1 kHz

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Instrumentation Amplifier (IA)

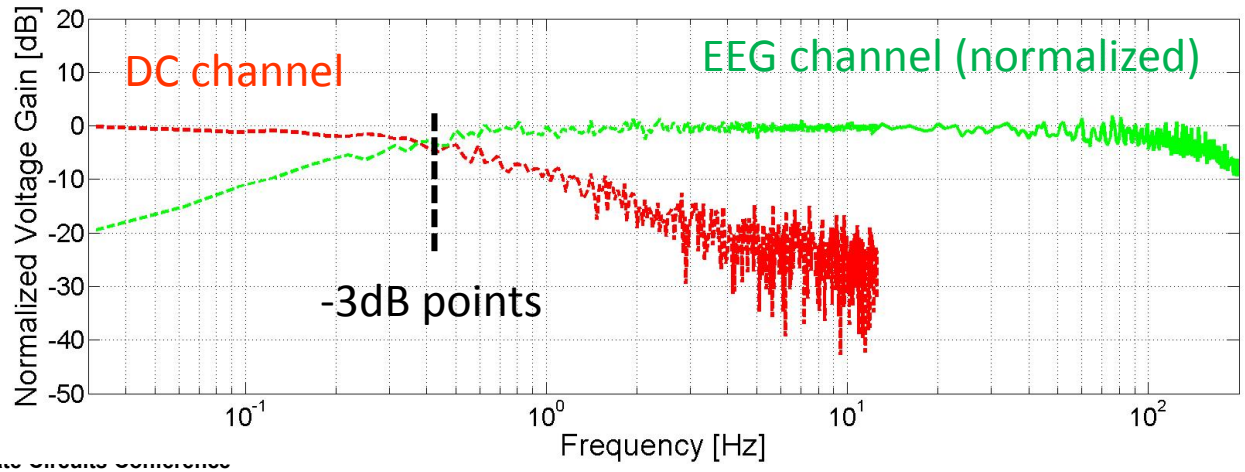


IA performance:

- ±350 mV offset tolerance
- 60nV/sqrt(Hz) @ ±350 mV
- 1 GΩ input impedance
- DC information available

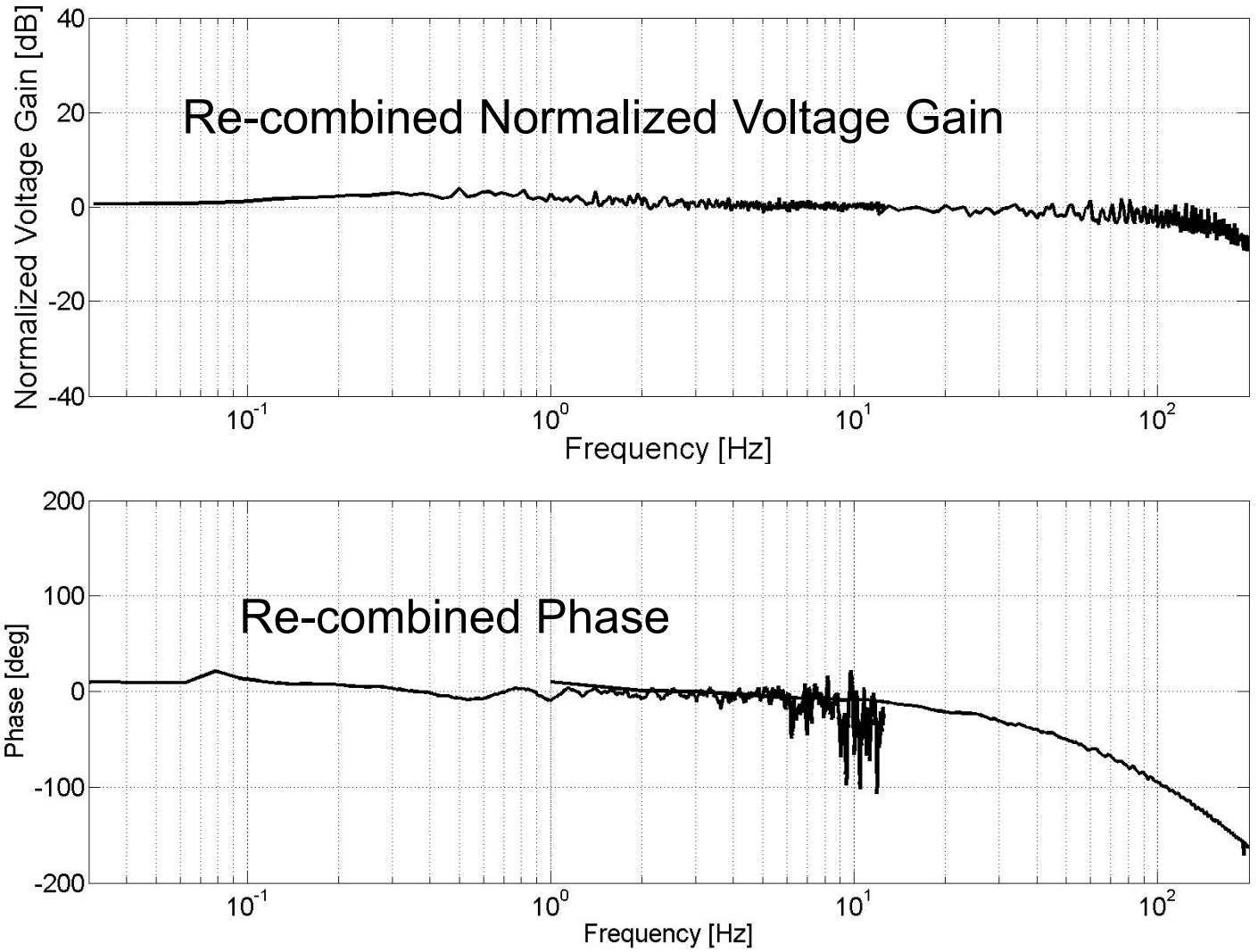
DC servo Loop

• V-to-V feedback, instead of V-to-I feedback in other bio-amplifiers



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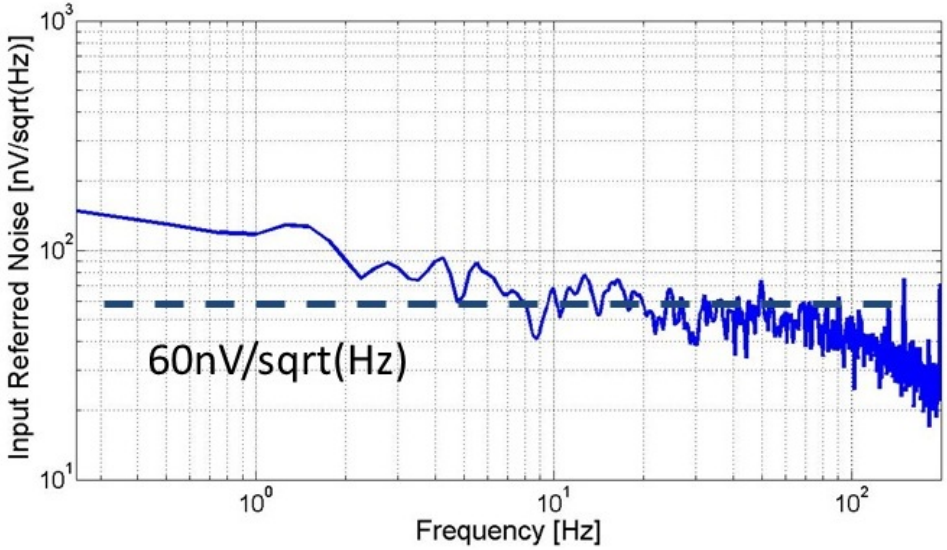
Functionally DC-coupled IA

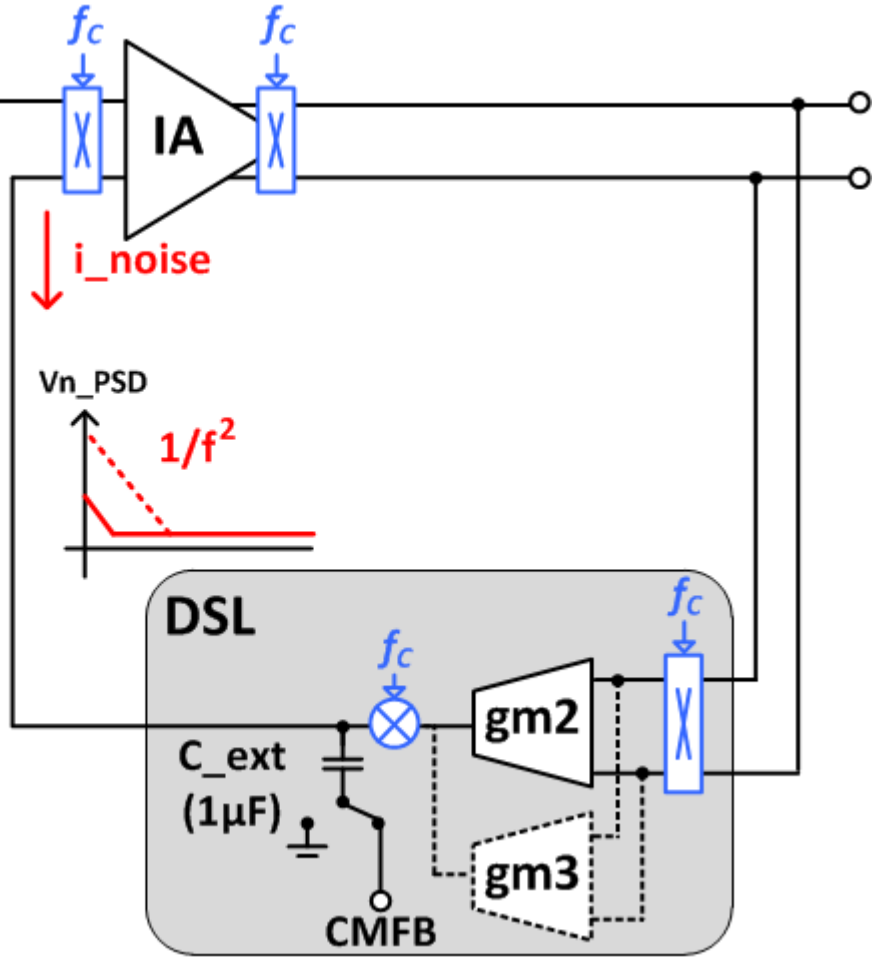


Reconstructed functionally DC-coupled IA with ±350mV DC input range

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Chopper Modulation for Low Noise



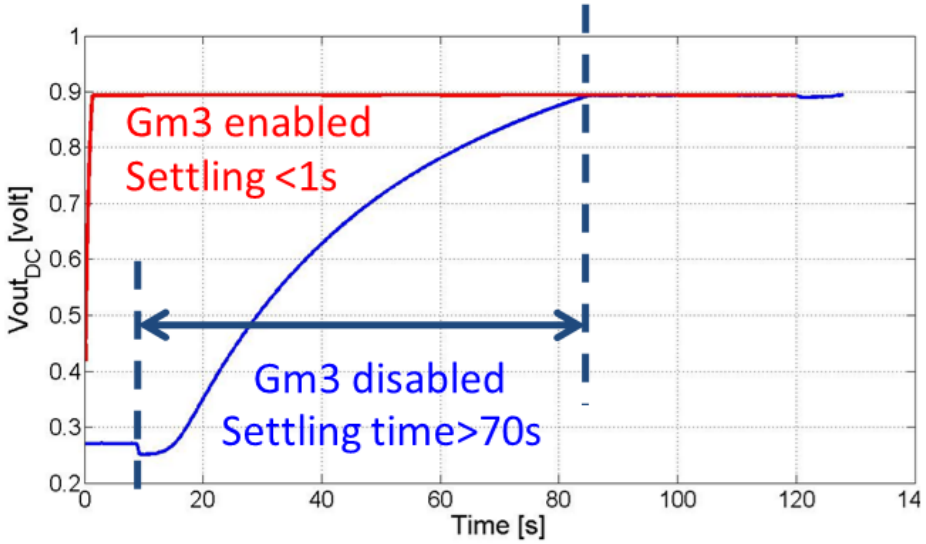


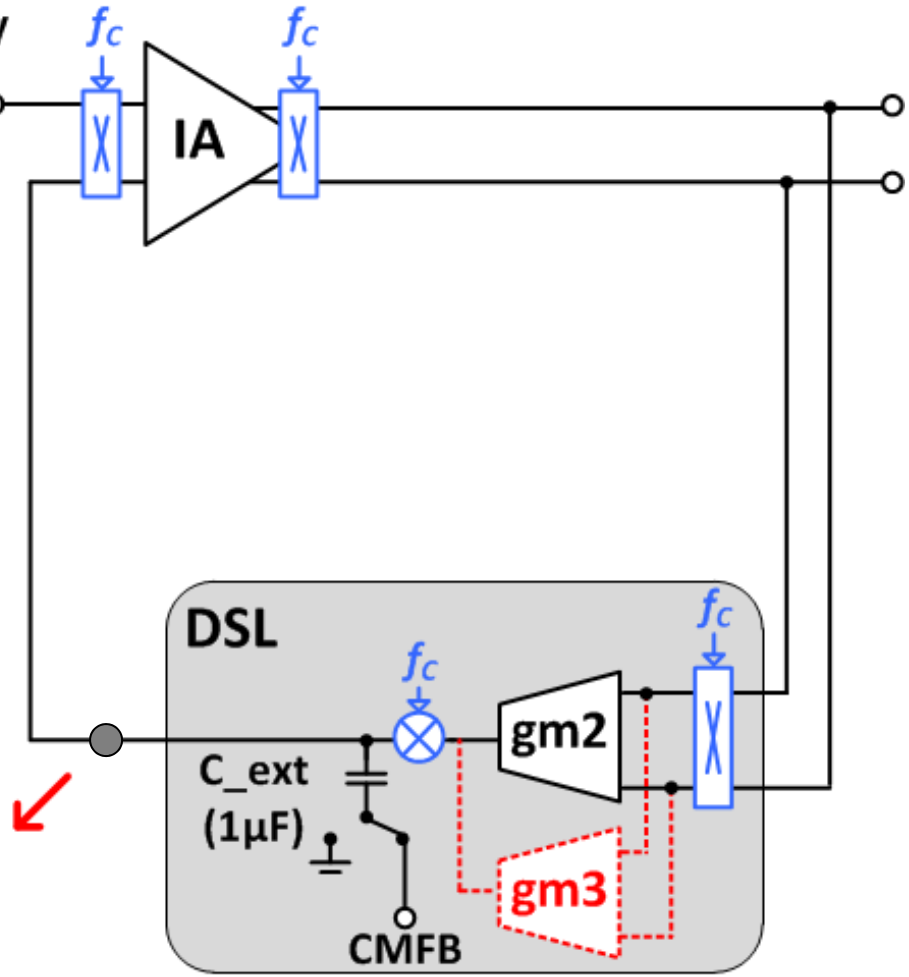
Relatively low impedance (C=1µF) at chopping node

→ Reduced $1/f^2$ noise

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Settling Time Reduction

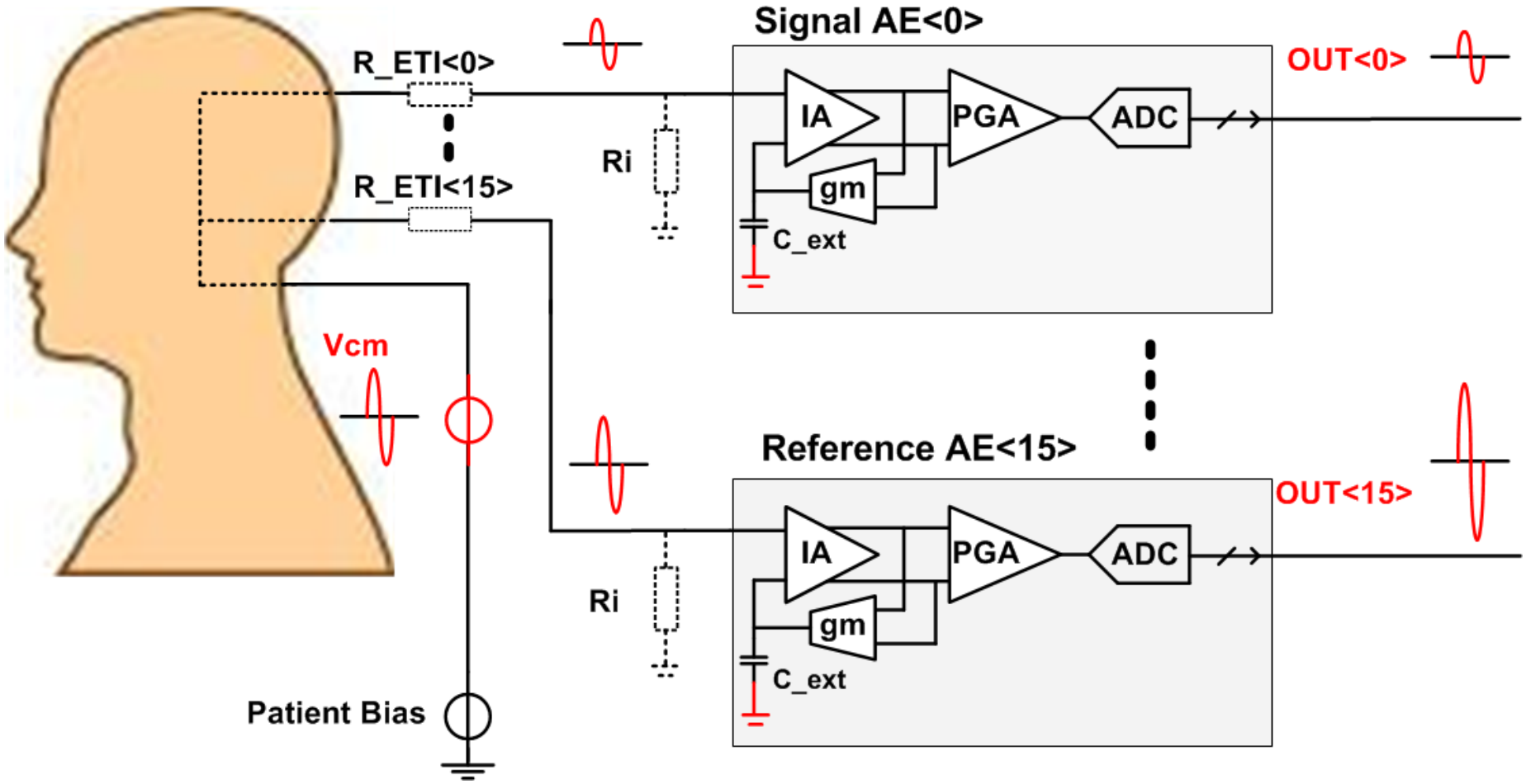




gm3 (=100*gm2) is temporarily switched on for fast start-up

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CMRR and Mismatches

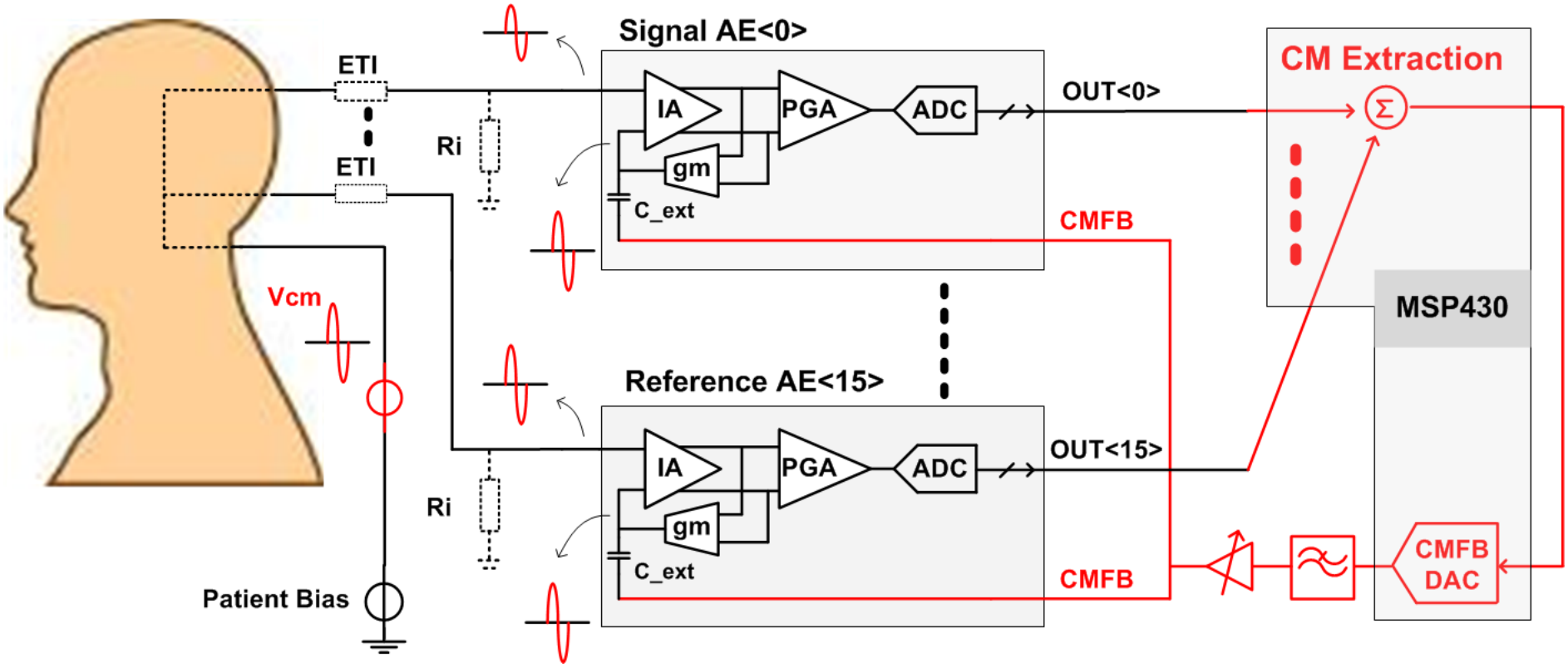


1. Component mismatch of Digital Active Electrodes
2. Electrode-Tissue Impedance (ETI) mismatch: $\Delta R_{ETI}/Ri$

→ <60dB CMRR. CM input also reduces output dynamic range

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Common-Mode Feedback (CMFB)

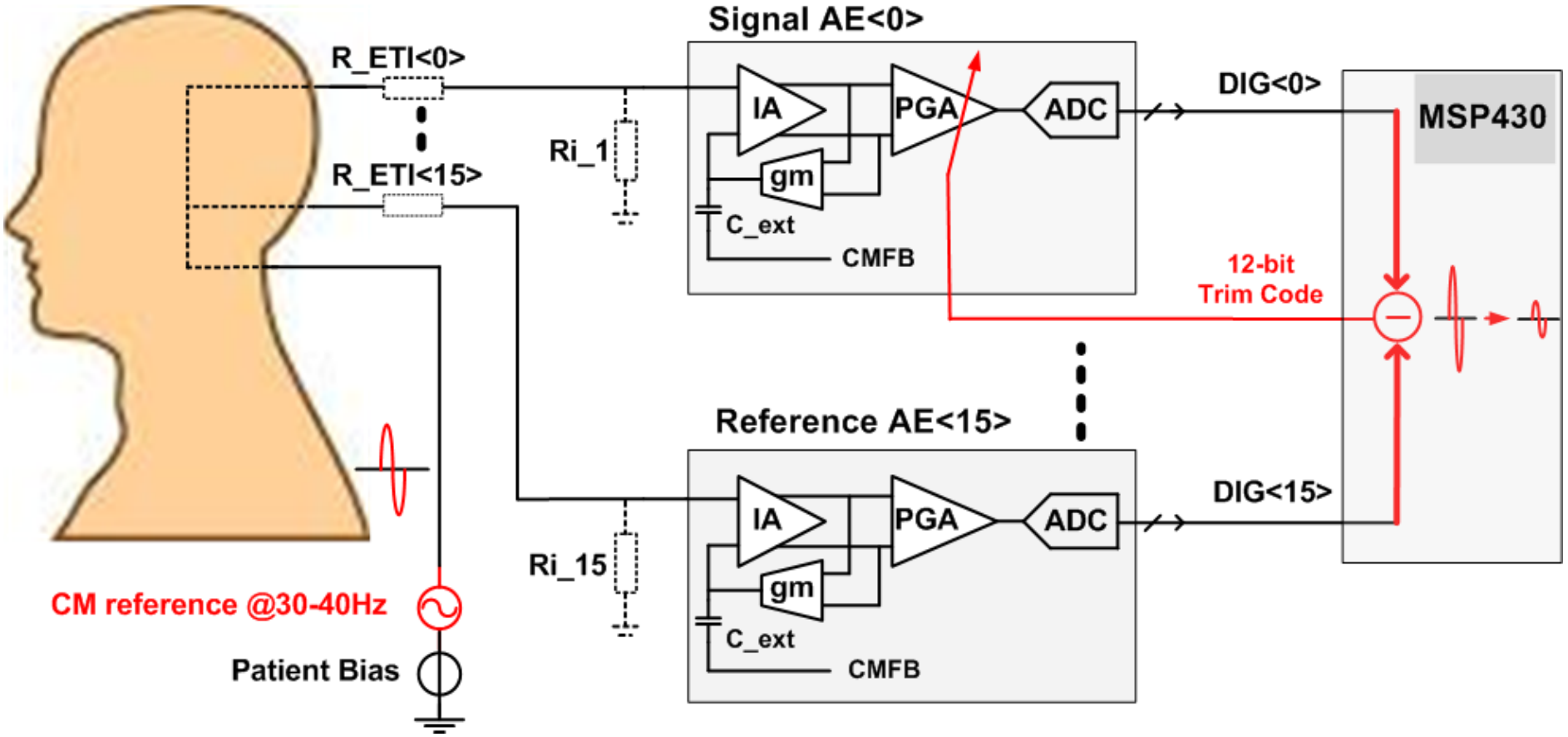


Averaging all outputs in MCU, feedback to each of the IA

- Reduce input CM swing of IA, CMRR boosted by 20*log (Av,CMFB)
- Minimize loop latency (due to I2C) for stability

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CMRR Trimming



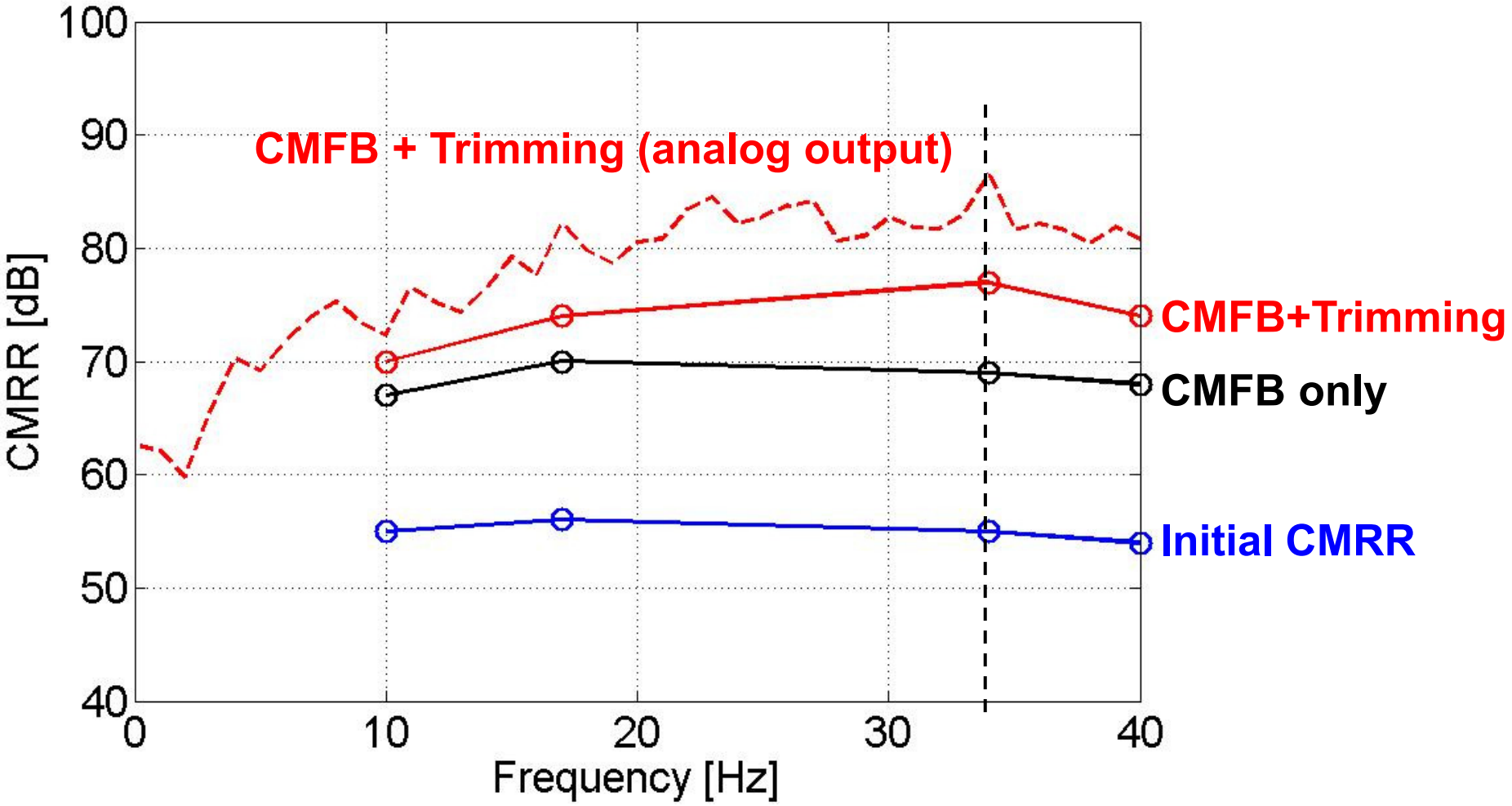
Trim the gain error in the foreground by adjusting PGA gain

→ Compensate up to 4.1% total mismatch

→ Accuracy determined by trim step and ADC resolution

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CMRR Measurement

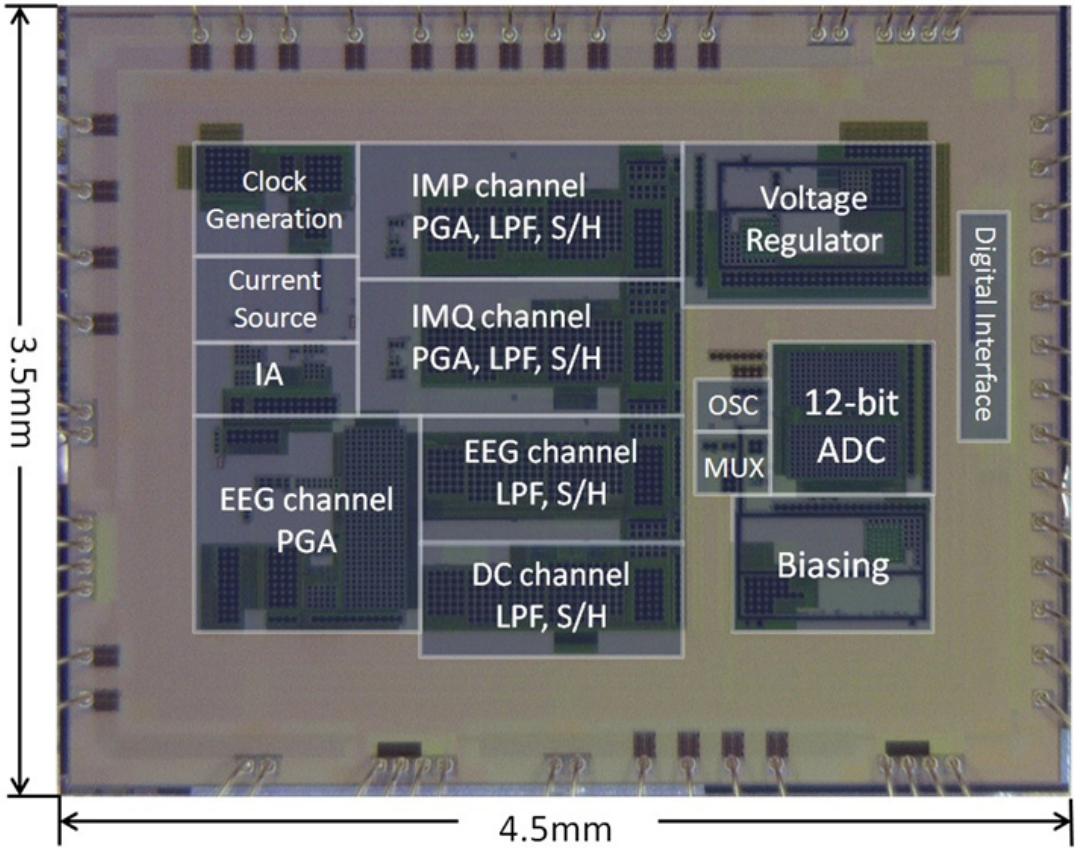


CMFB + digital trimming: CMRR from 55 dB to 77 dB

CMFB + analog trimming: maximum 85 dB CMRR

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Chip Photograph

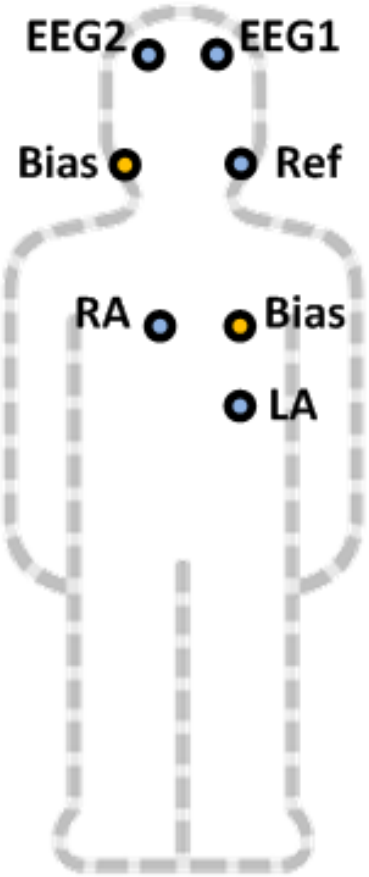


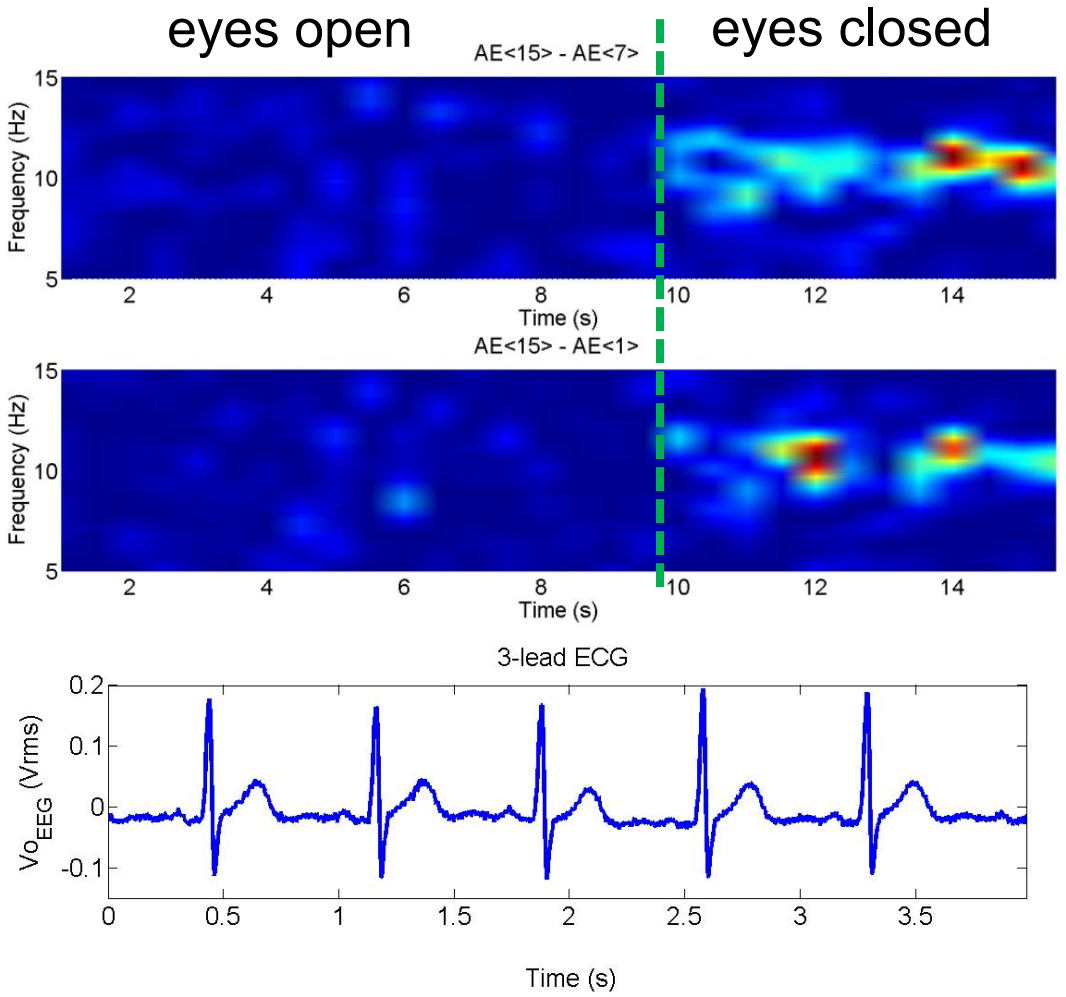
	This work
Input impedance	1 GΩ
Input-referred noise/channel	0.65 µVrms (0.5-100 Hz)
Electrode Offset	±350 mV
CMRR	77-85 dB
Current /channel	150 µA
DC-coupled ExG	yes
ETI Measurement	yes
Digital interface	I2C

- Standard 0.18µm CMOS process, 1.8 V core supply
- 3.5mm*4.5mm chip area
- Performance competitive with state-of-the-art

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Biopotential Measurement





2-channel EEG using dry electrodes

1-lead ECG using wet electrode

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Conclusions

A Digital Active Electrode ASIC for Portable/Wearable EEG System

- Amplifiers, ADC, I2C integrated on a single chip: Low Cost
- 4-wire bus interfacing to standard MCU: Modularity
- Low-noise DC-coupled IA, CMRR improvement: Signal Quality
- Dry electrodes: User Comfort

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Thank You!

Questions?

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An Analog-Digital-Hybrid Single-Chip RX Beamformer with Non-Uniform Sampling for 2D-CMUT Ultrasound Imaging to Achieve Wide Dynamic Range of Delay and Small Chip Area

***Ji-Yong Um*[1]**, *Yoon-Jee Kim[1], Seong-Eun Cho[1], Min-Kyun Chae[1], Jongkeun Song[2], Baehyung Kim[2], Seunghun Lee[2], Jihoon Bang[2], Youngil Kim[2], Kyungil Cho[2], Byungsub Kim[1], Jae-Yoon Sim[1], Hong-June Park[1]*

[1] POSTECH, Korea

[2] SAIT, Korea

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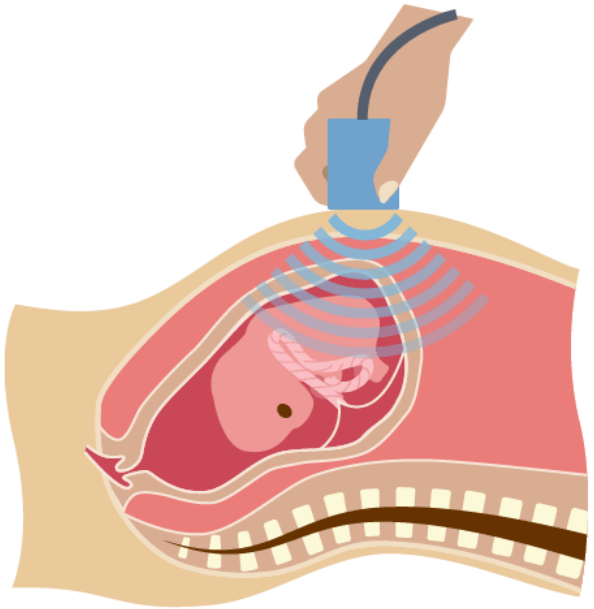
Outline

- Introduction
- Proposed schemes
- Circuit implementations
- Measurements
- Conclusion

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Ultrasound Medical Imaging

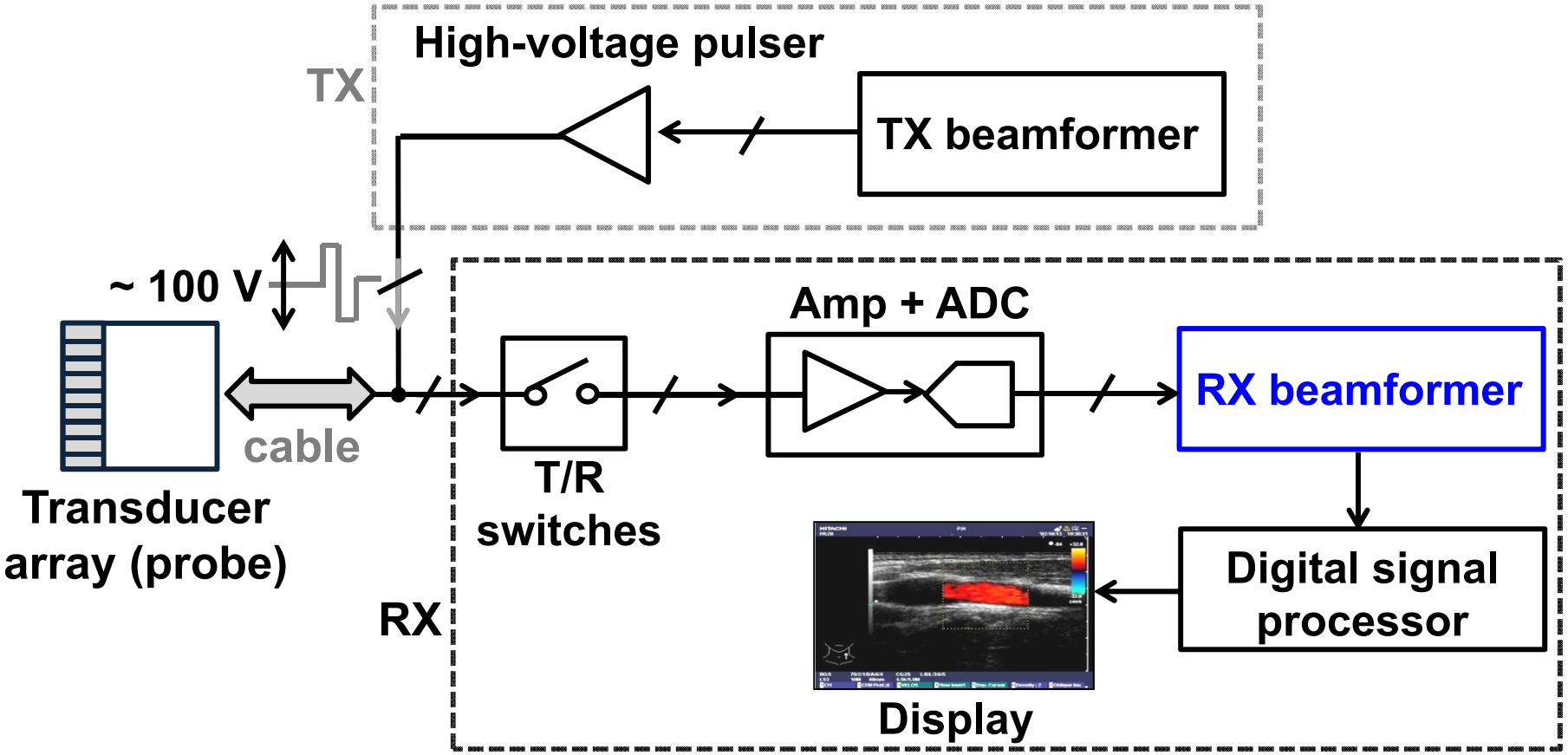




- **Image : cross-section of inner organs**
- **Feature (compared to X-ray, CT, MRI, and PET)**
 - Safe
 - Relatively inexpensive
 - Real-time

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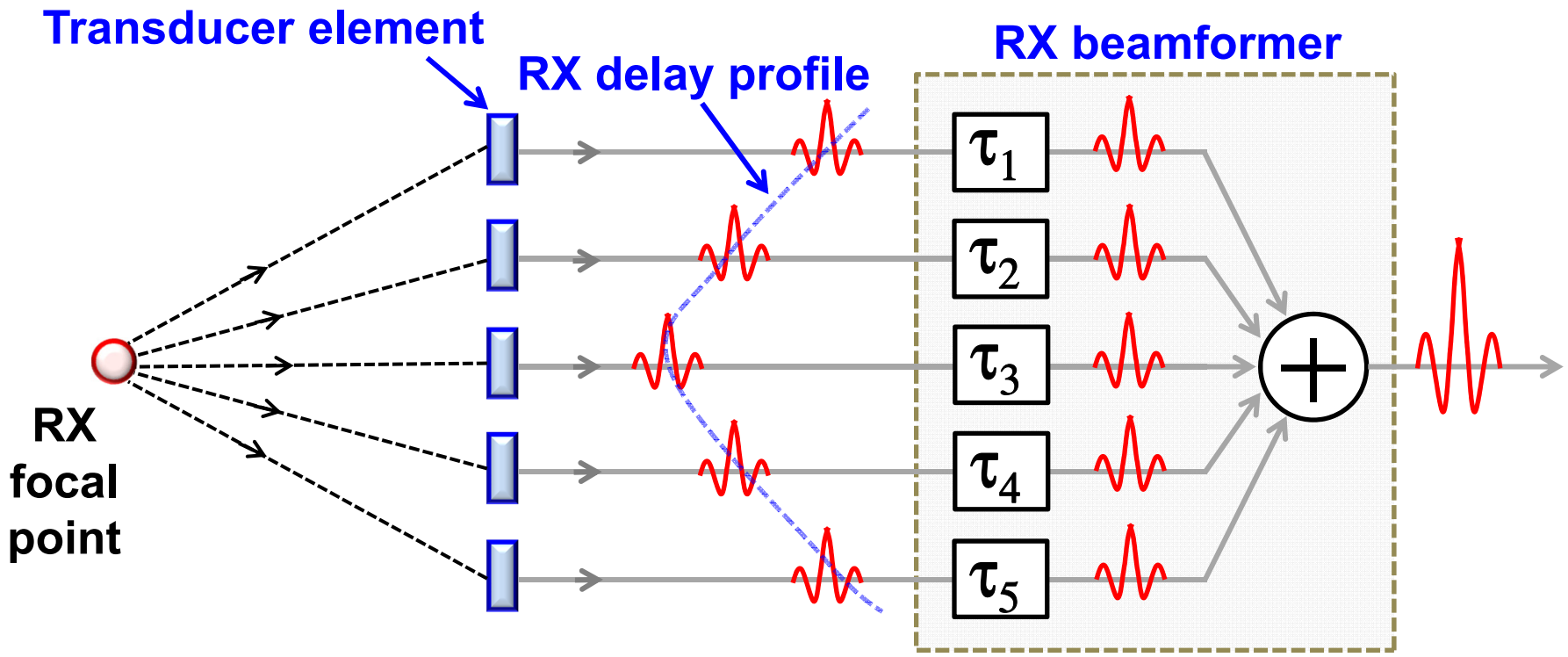
Conventional US Machine



- Consists of probe, TX, RX
- This work : a small-area single-chip RX beamformer

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RX Beamforming



- **Beamforming = focusing**
- **RX beamformer compensates for RX delay profile**

➔ desired signal ↑, undesired noise and side-lobe ↓

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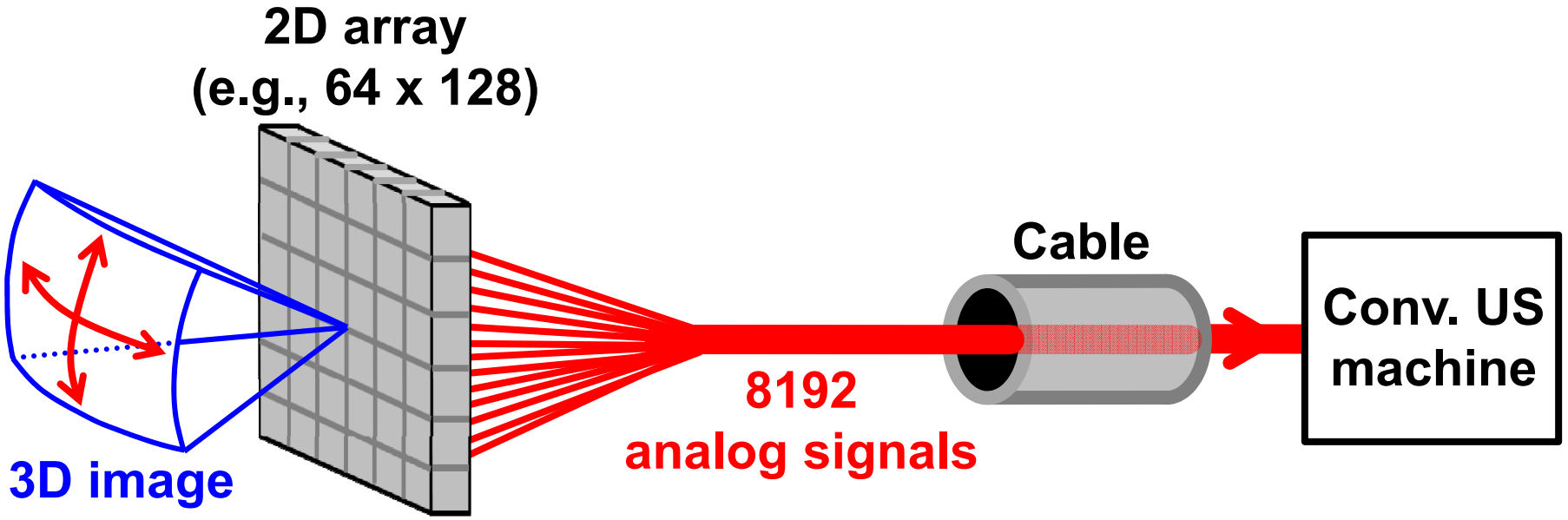
Conventional RX Beamformer

- **Digital beamformer**
 - the most widely used for good image quality
 - requires 1 ADC for 1 channel

➔ ***Difficult*** to use with **2D transducer array**

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Limitation of DBF in 2D Array



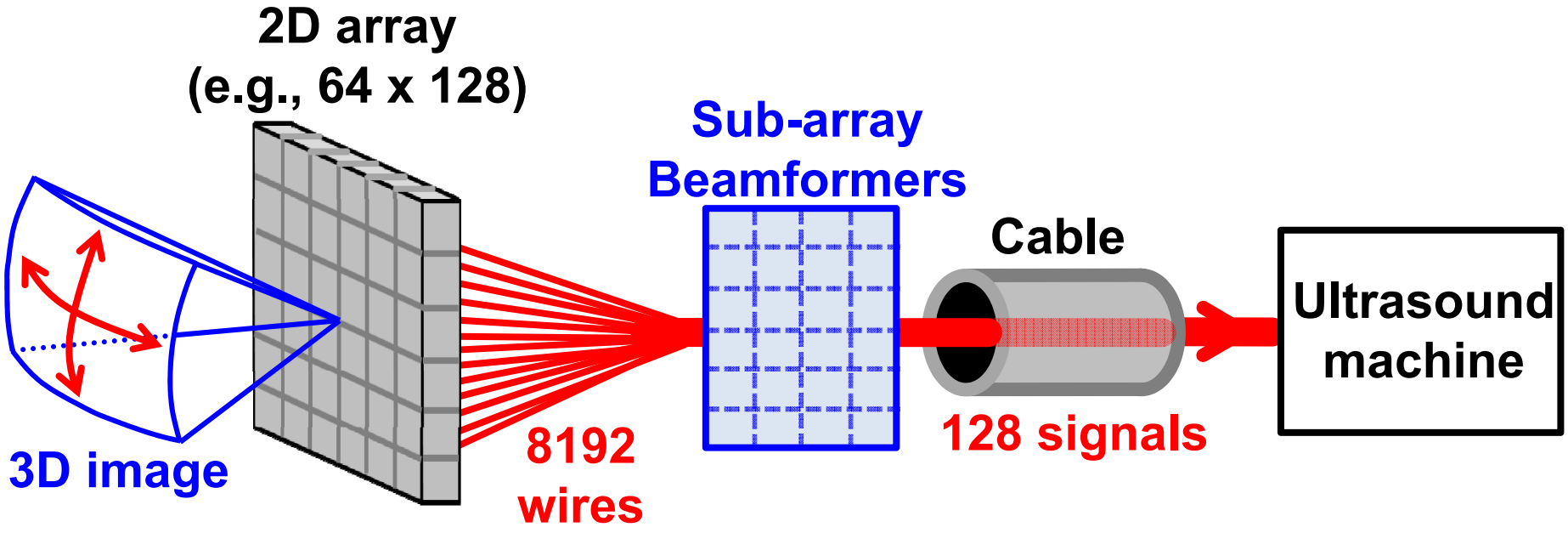
- **2D transducer array is used to get 3D image**

 e.g., 64 x 128 2D CMUT array
- **If DBF is used, it requires tremendous # (e.g., 8192) of ADCs and wires for analog signals**

 ➔ impossible to implement with current technology

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Sub-Array BF for 2D Array



- **128 SA BF convert 8192 echo signals into 128 signals**
 - One SA BF accepts either 8 x 8 or 64 x 1 elements
 - Conventional SA BF is analog beamformer
 - **This work : analog-digital-hybrid SA BF**

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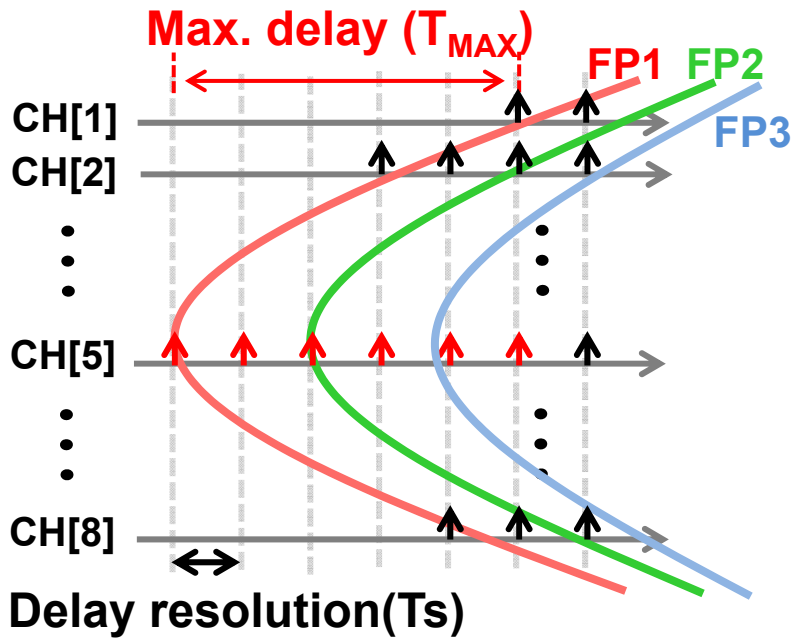
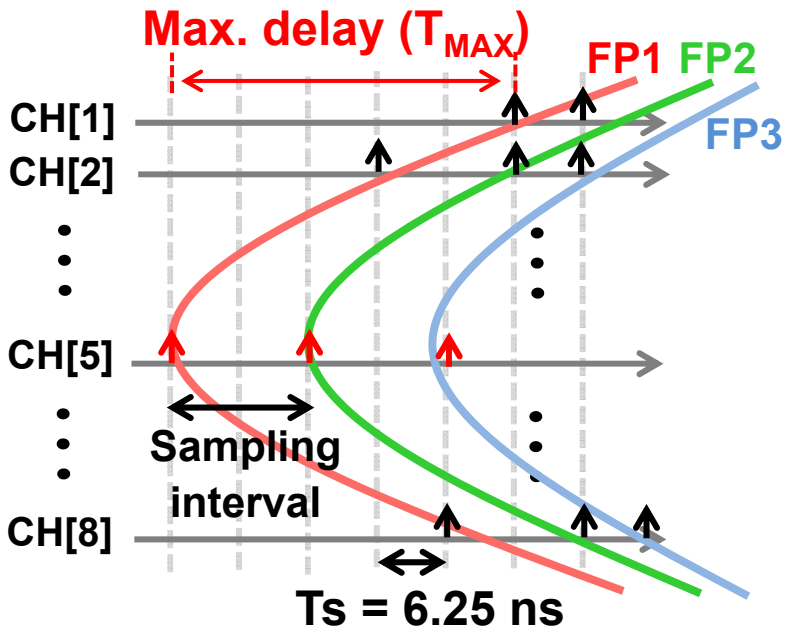
This Work

- **Target : 1 x 64 sub-array beamformer**
 - Max. delay (T_{MAX}) 8 μs, delay resolution (Ts) 6.25 ns
 - Large T_{MAX} / T_S ➔ large memory

- **Proposed schemes**
 - **1) Non-uniform sampling** ➔ reduces memory size
 - **2) Hybrid (analog + digital) beamformer**
 ➔ further reduces memory area

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Non-Uniform BF

	Uniform sampling	Non-Uniform sampling
Concept		
Memory size / CH (= L_{MAX})	T_{MAX} / T_S	T_{MAX} / dominant sampling interval

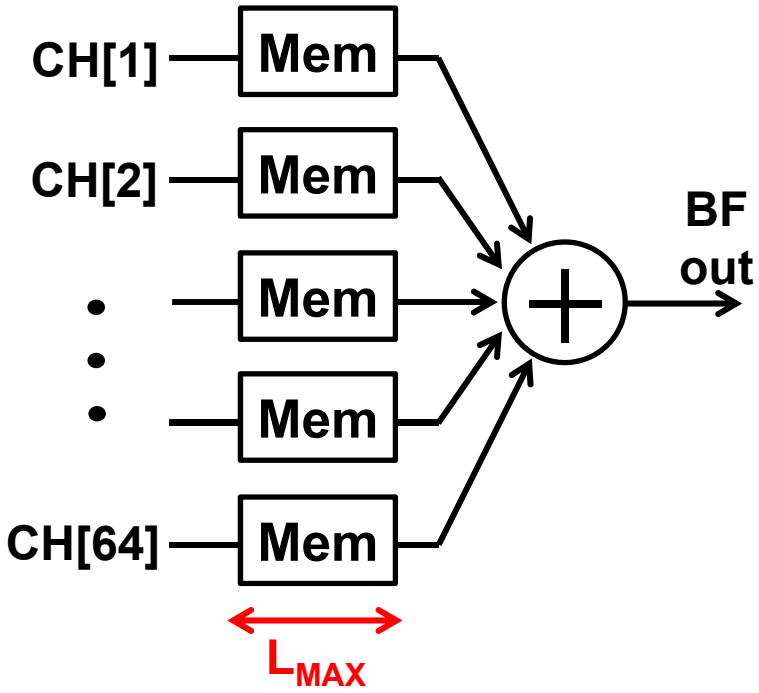
- **Non-uniform BF samples at the delay profile points only**
- **Dominant sampling interval of this work = 8Ts**

➔ non-uniform sampling BF requires ***8 times smaller mem. size !***

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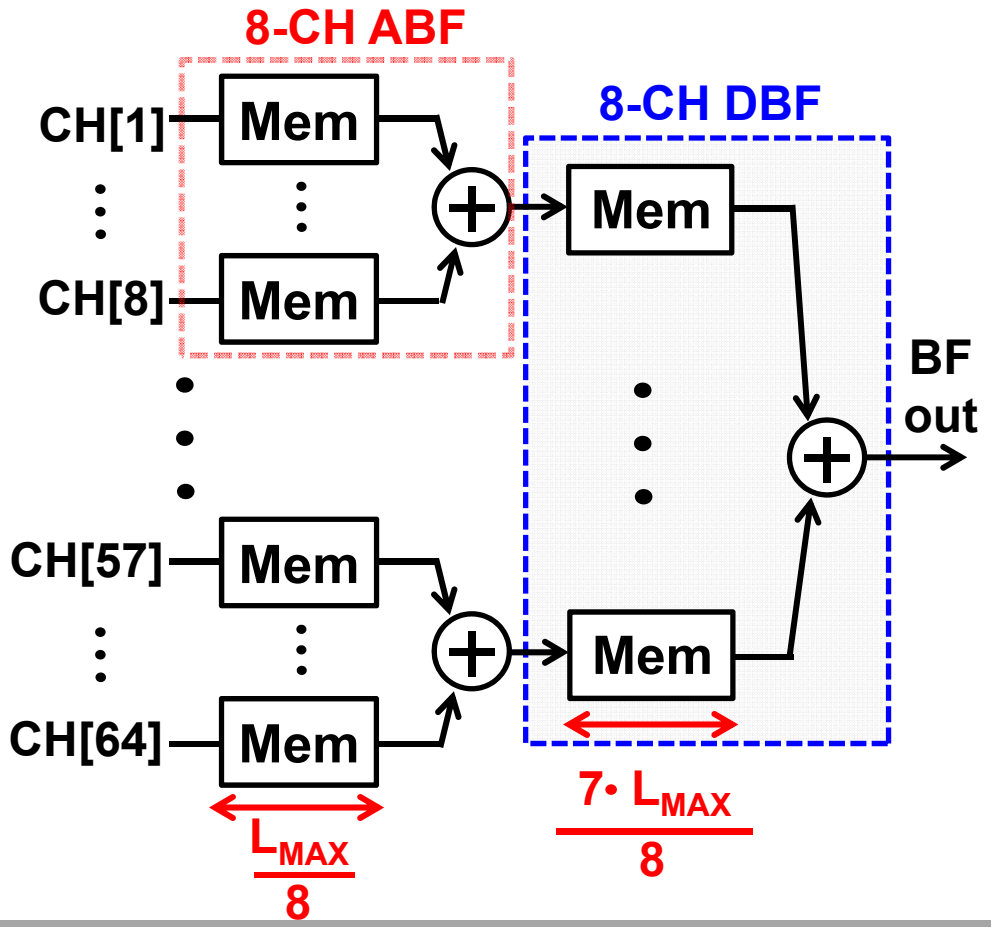
Two-Stage BF

Single-Stage BF



: Mem. size for max. delay T_{MAX}

Two-Stage BF (HBF)



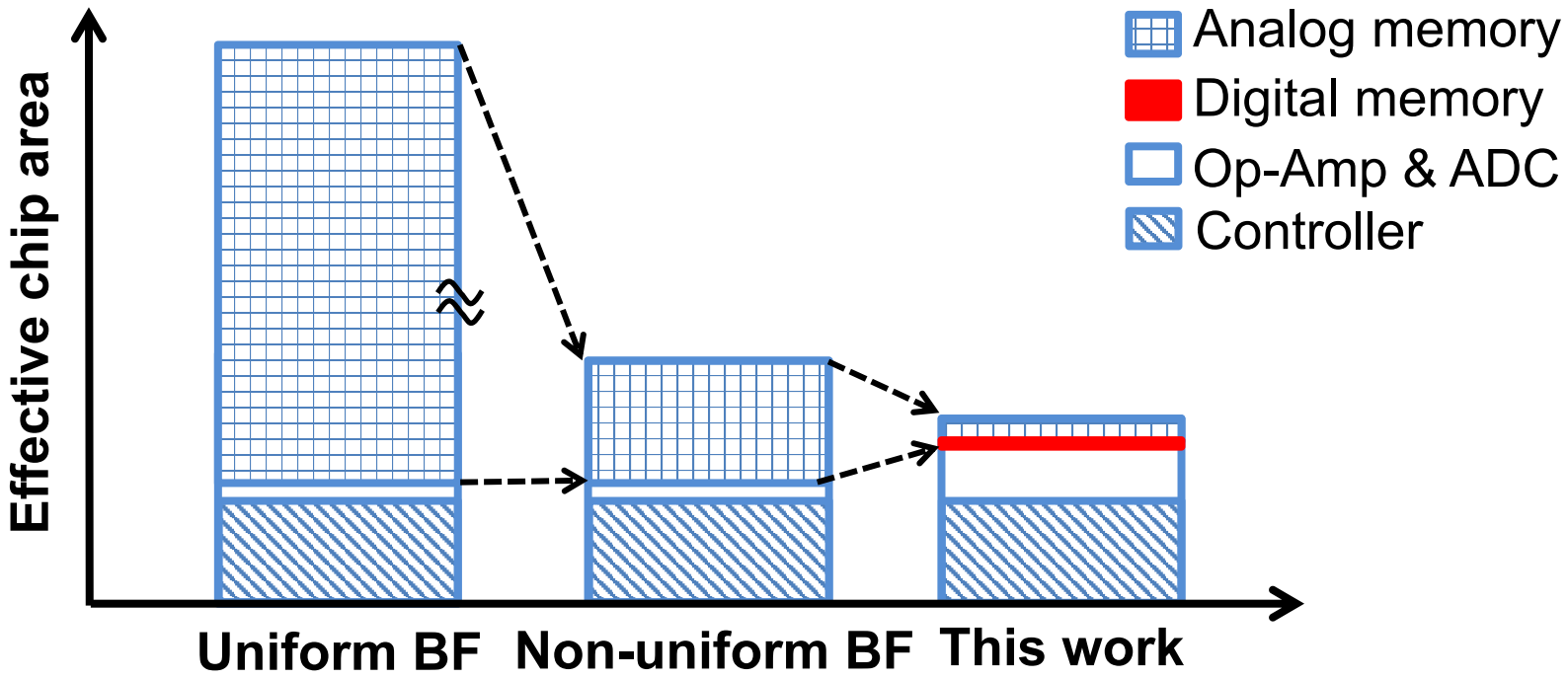
Total mem. size

Single-Stage BF: $64 \times L_{MAX}$

Two-Stage BF (HBF): $64 \times \frac{L_{MAX}}{8} + 8 \times \frac{7 \cdot L_{MAX}}{8} = 15 \times L_{MAX}$

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Comparison of Memory Size



- **Reduction factor**
 - Non-uniform sampling scheme : 8
 - Two-stage (hybrid) architecture : ~ 4

 ➔ ~ 30 times smaller than uniform sampling BF

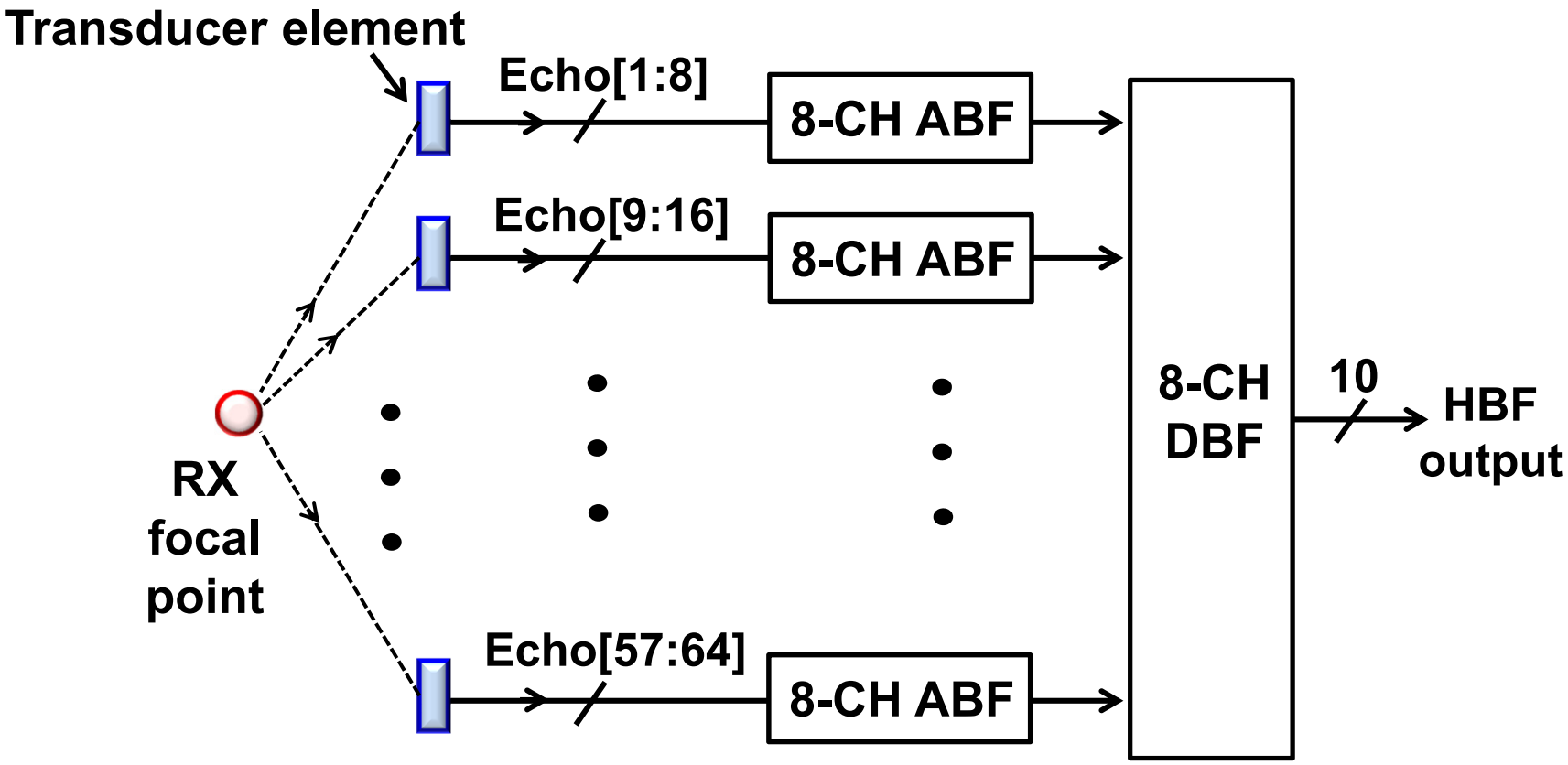
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Outline

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Proposed Hybrid Beamformer

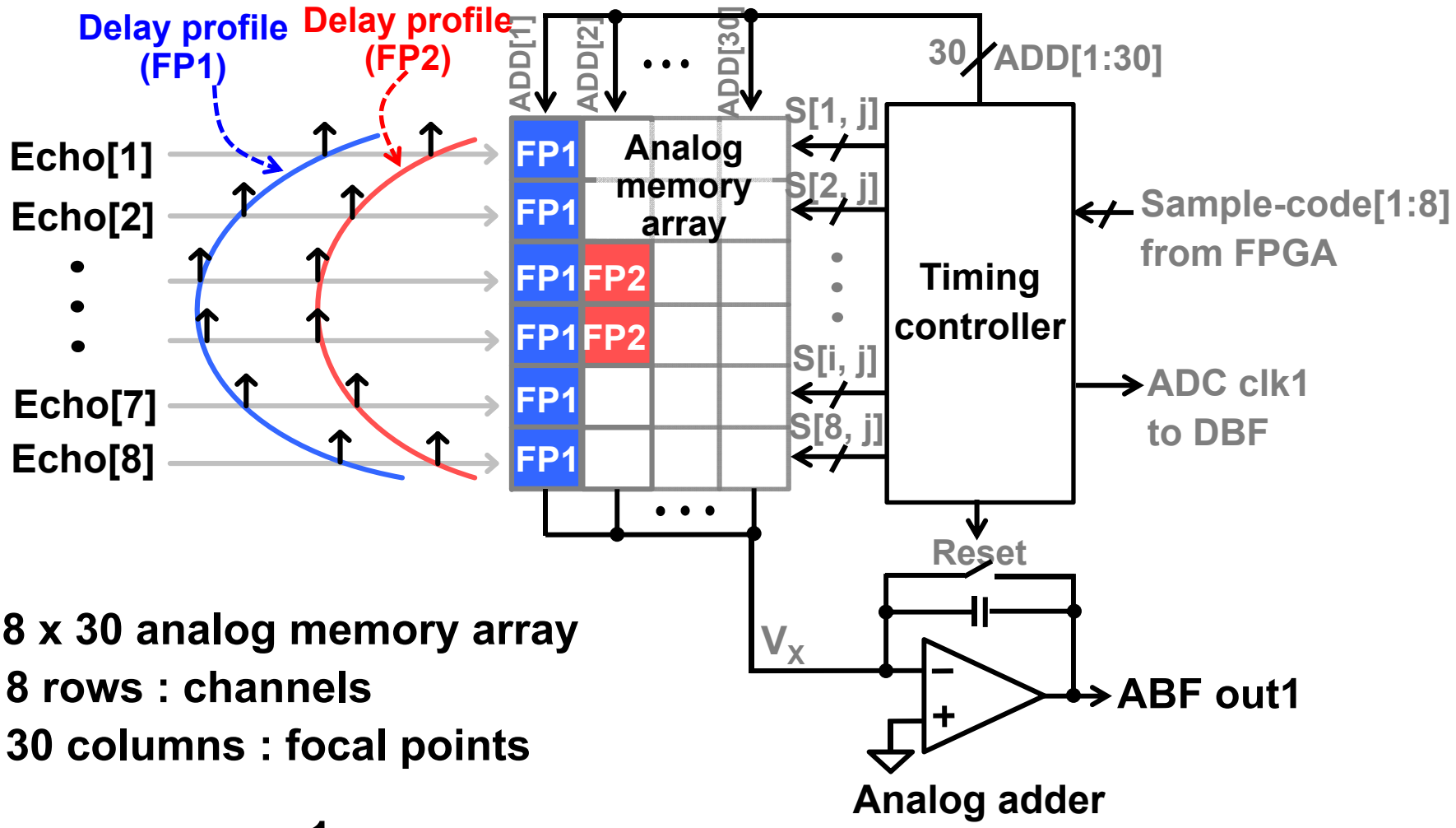


- 8 ABFs + 1 DBF
- Delay range

$$\text{- ABF : } \frac{1}{8} \cdot T_{MAX} \text{ (= 1 } \mu\text{s)} \qquad \text{- DBF : } \frac{7}{8} \cdot T_{MAX} \text{ (= 7 } \mu\text{s)}$$

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8-CH ABF (Analog BF, 1/3)

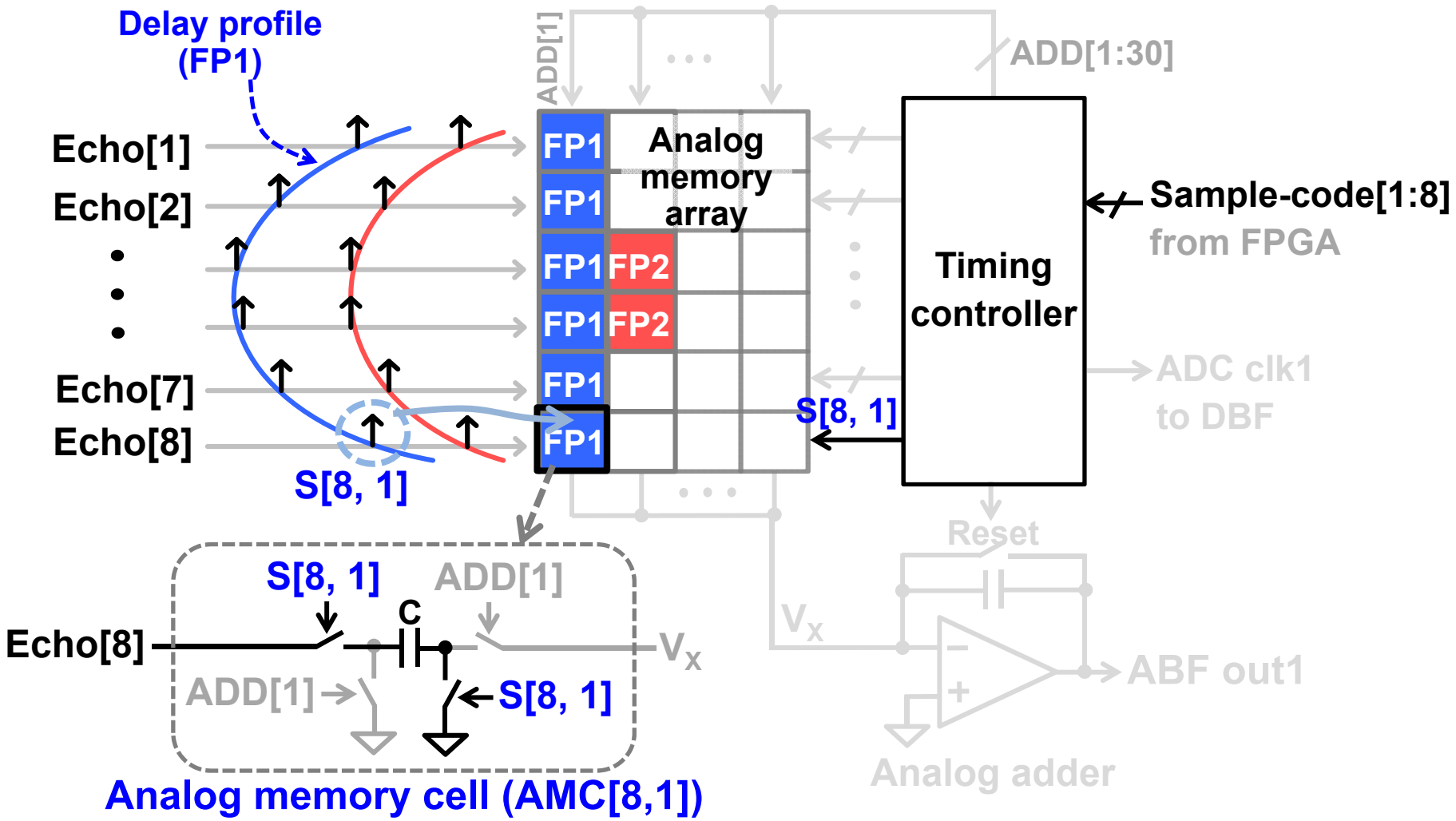


- 8 x 30 analog memory array
 - 8 rows : channels
 - 30 columns : focal points

- # columns = $\frac{1}{8} \cdot L_{MAX}$ x 1.5 (50% margin)

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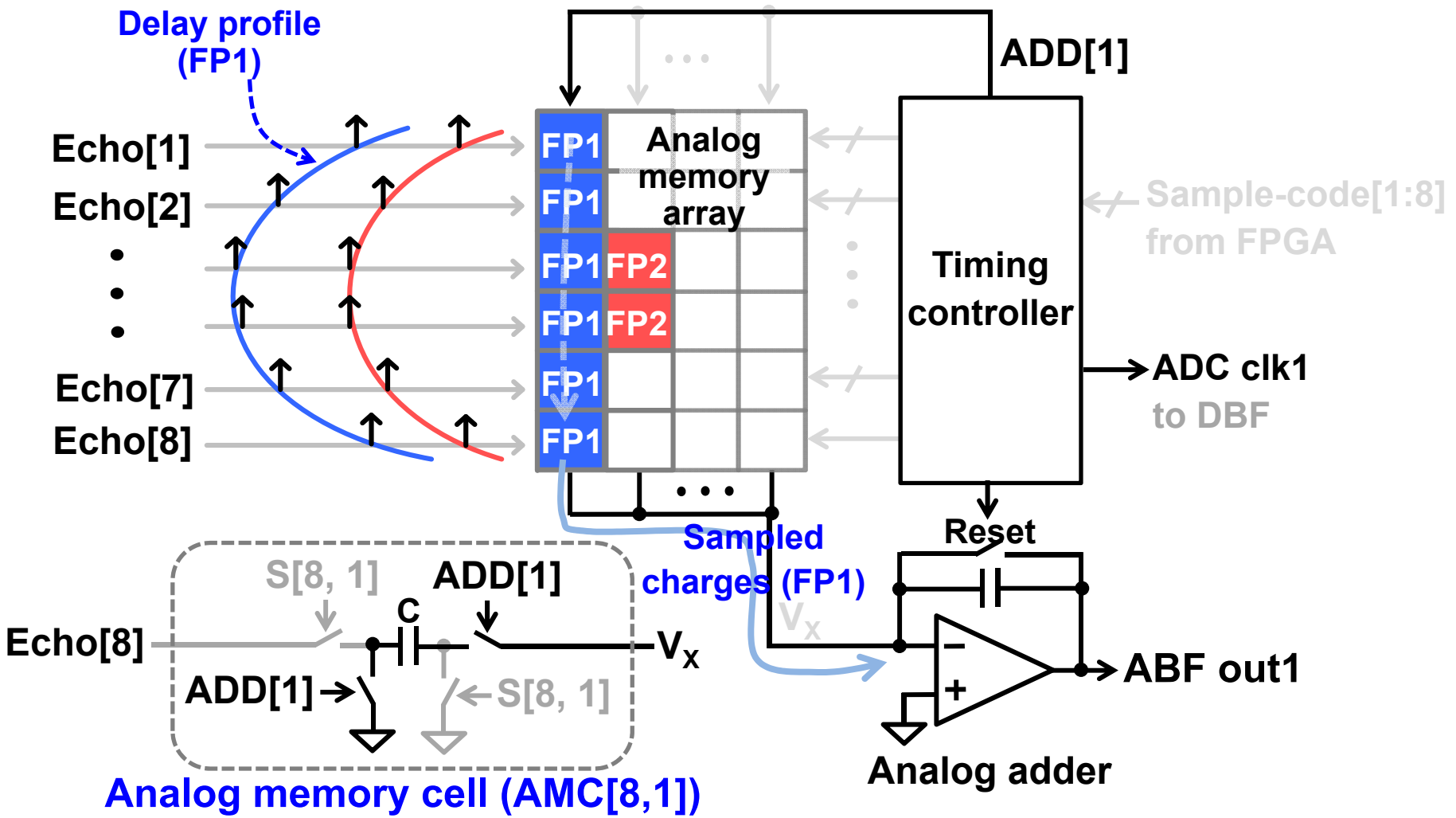
8-CH ABF (Analog BF, 2/3)



- AMC[8,1] samples echo[8] at delay profile point (S[8,1])

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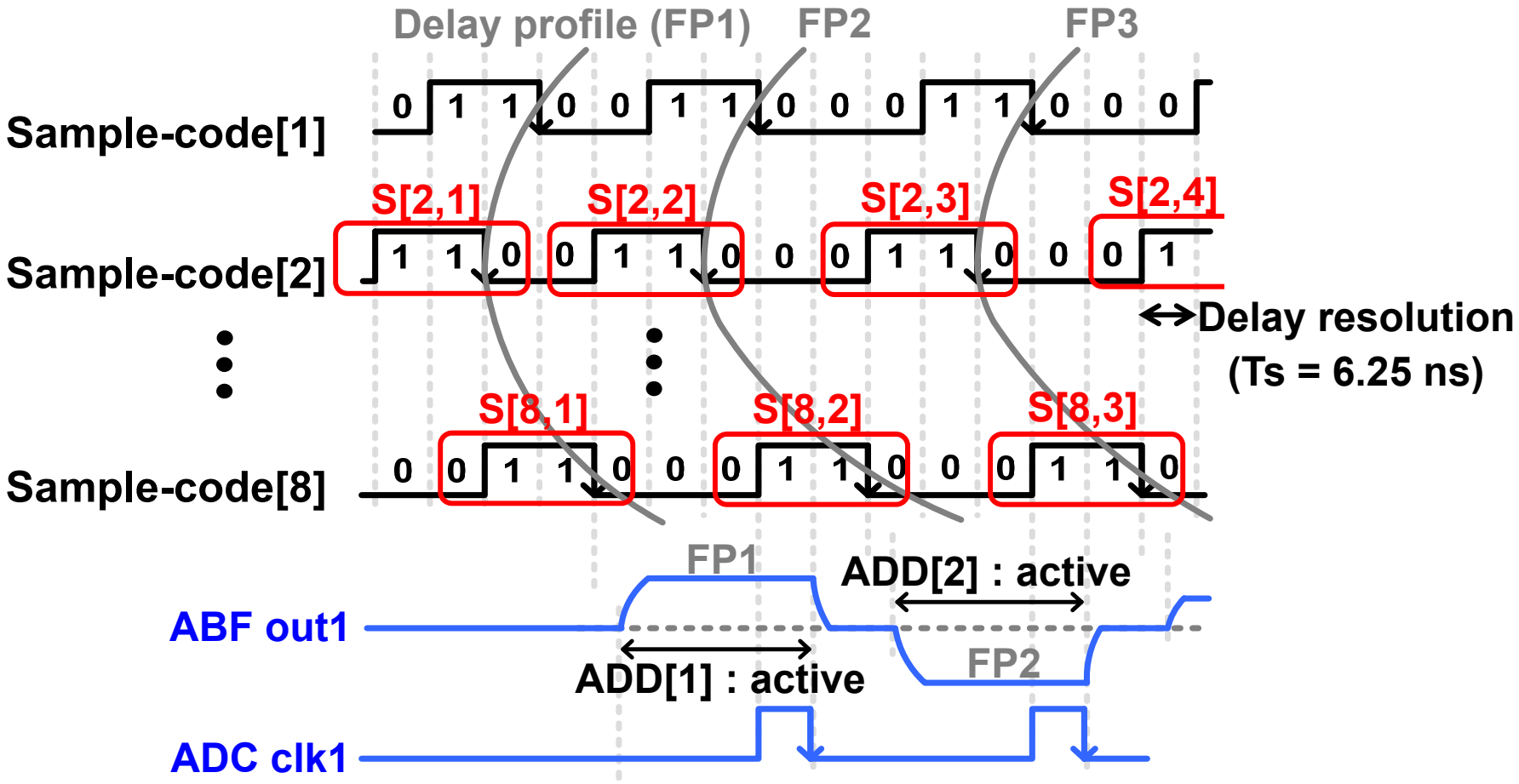
8-CH ABF (Analog BF, 3/3)



- After completing FP1 sampling, all FP1 signals(AMC[i,1]) are added

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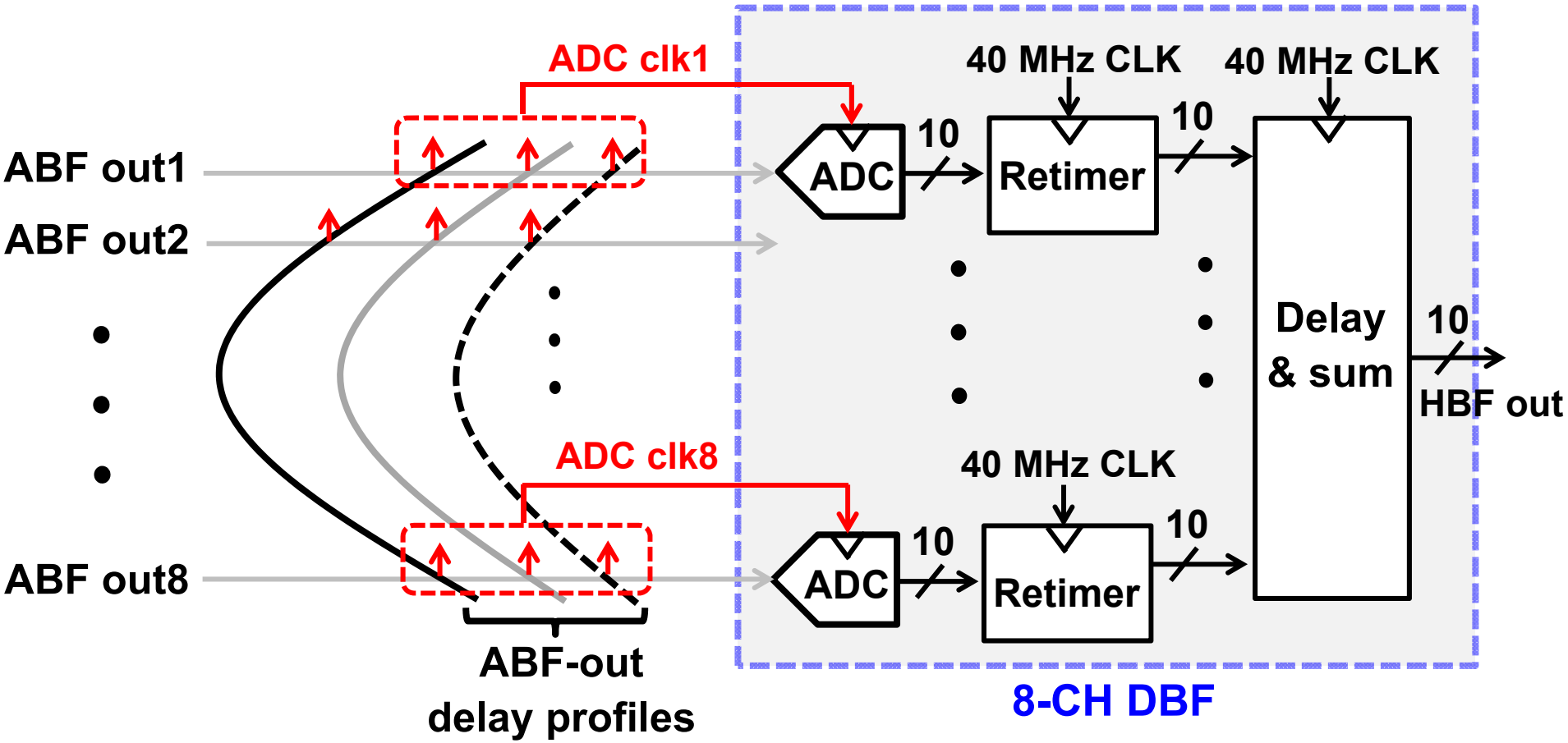
Sample & Add Operation of ABF



- ADD[j] enables the addition of the j-th focal point FP_j signals
- ABF output is sampled by ADC at the falling edge of ADC clk1

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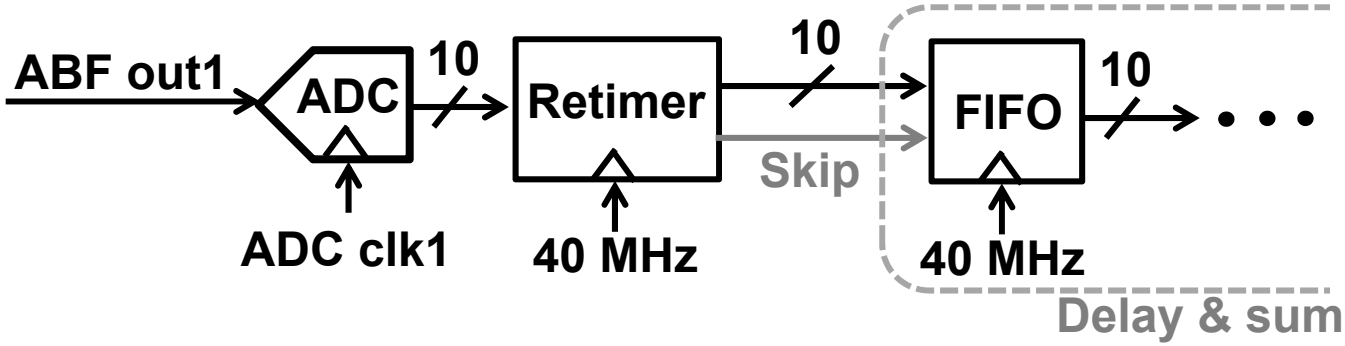
Interface between 8 ABFs and DBF



- **Each ABF output is A/D converted by an ADC within 8-CH DBF**
- **Sampling interval : non-uniform in time**
 - any value between 25 ns and 50 ns in 6.25-ns step

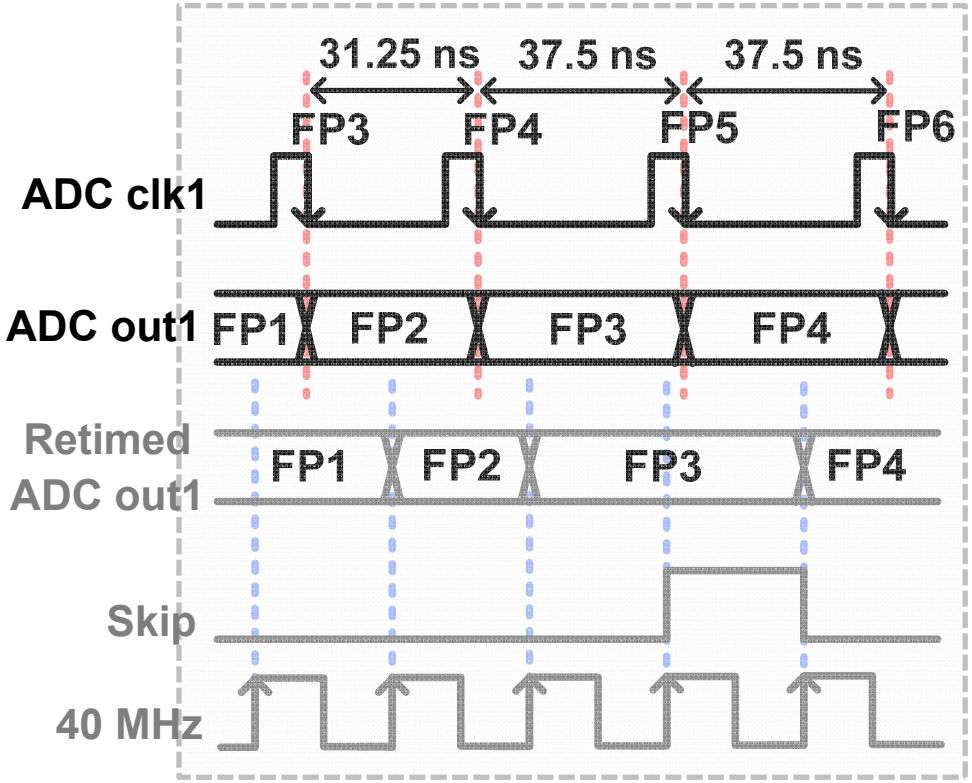
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Retiming ADC Output



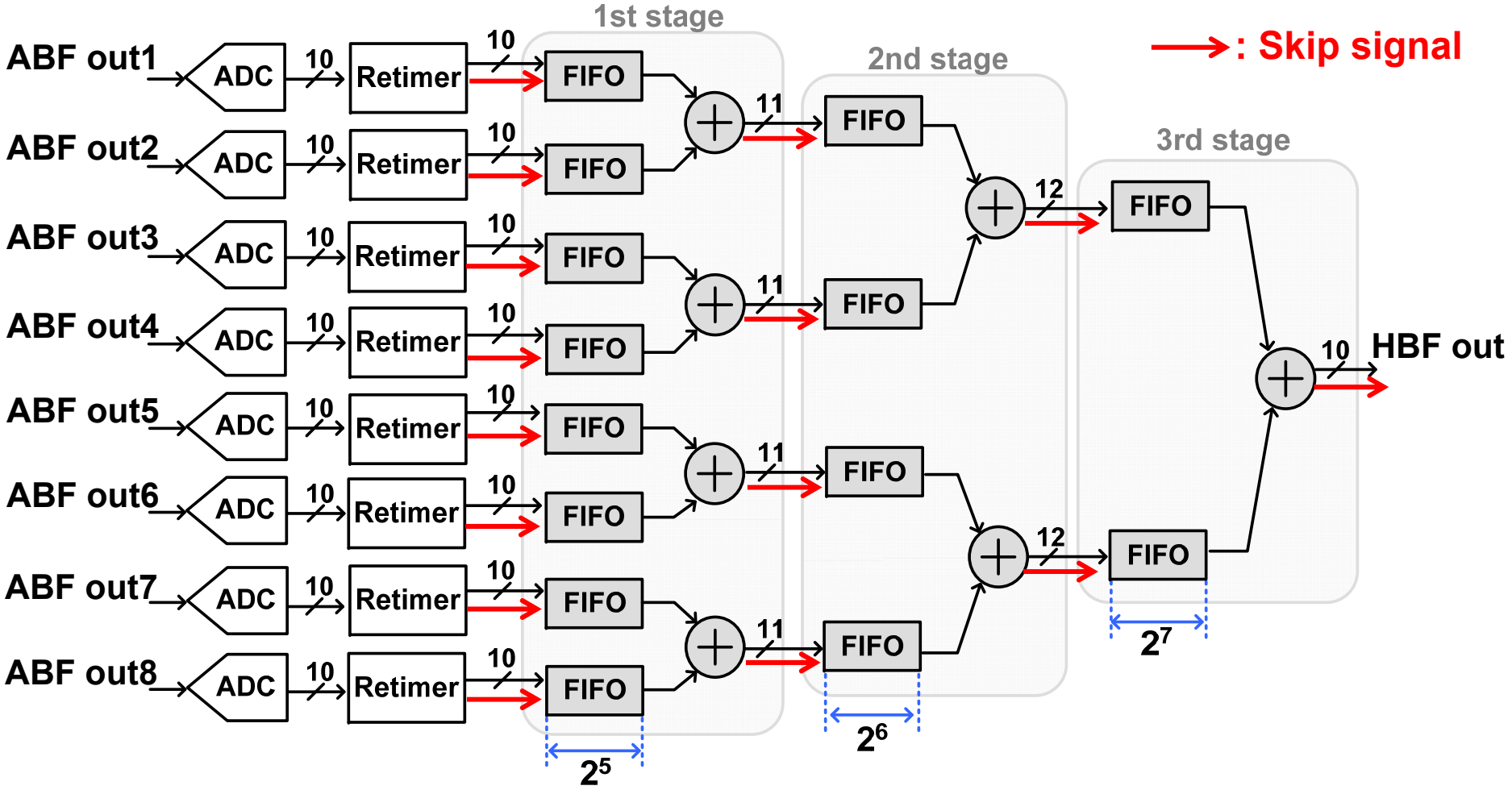
- Retime *ADC out1* with 40 MHz clk
- *Skip* signal prohibits FIFO input of *Retimed ADC out1*

➔ ***Simple FIFO control !***



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8-CH DBF



- **Delay & sum : 3-stage FIFO** reduces FIFO size (8.45-kbits)
- **All blocks except ADC work at 40 MHz**

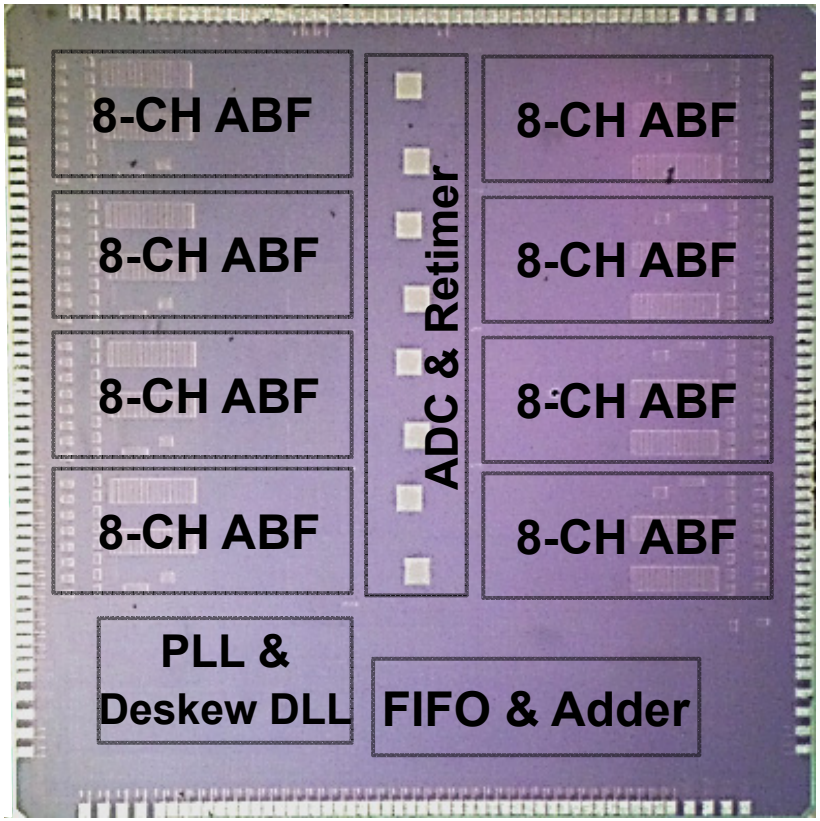
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Outline

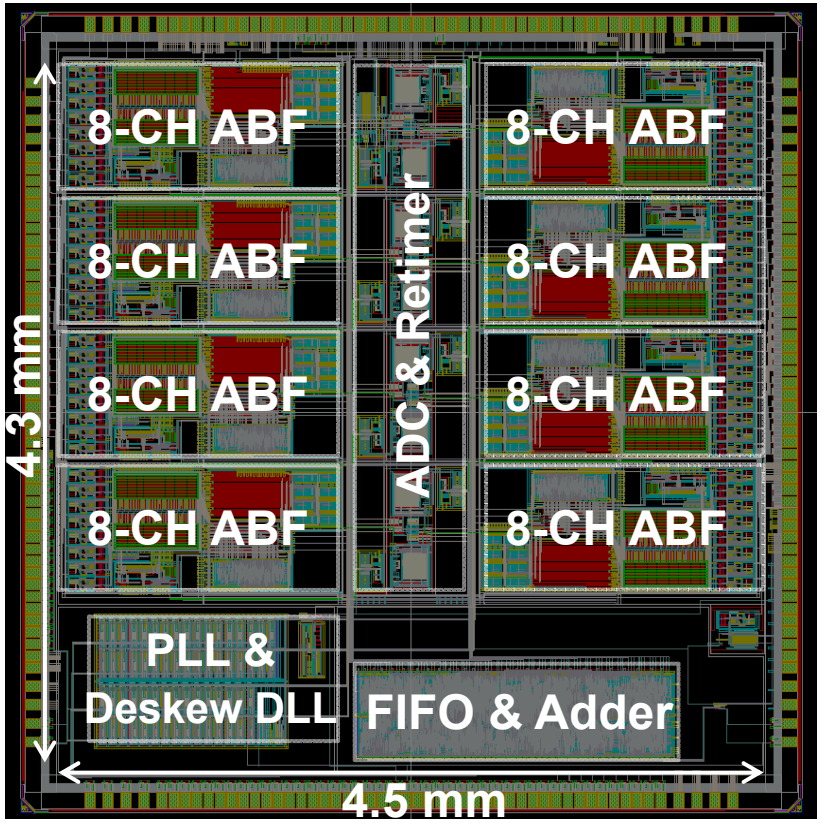
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 - **6CH echo emulation**
 - **64CH echo emulation**
 - **B-mode image with CMUT probe**
- Conclusion

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Chip Micrograph & Layout



Micrograph



Layout

- Process : 0.13 μm CMOS
- Total area : 19.4 mm^2
- The effective area of core circuit : 8.52 mm^2

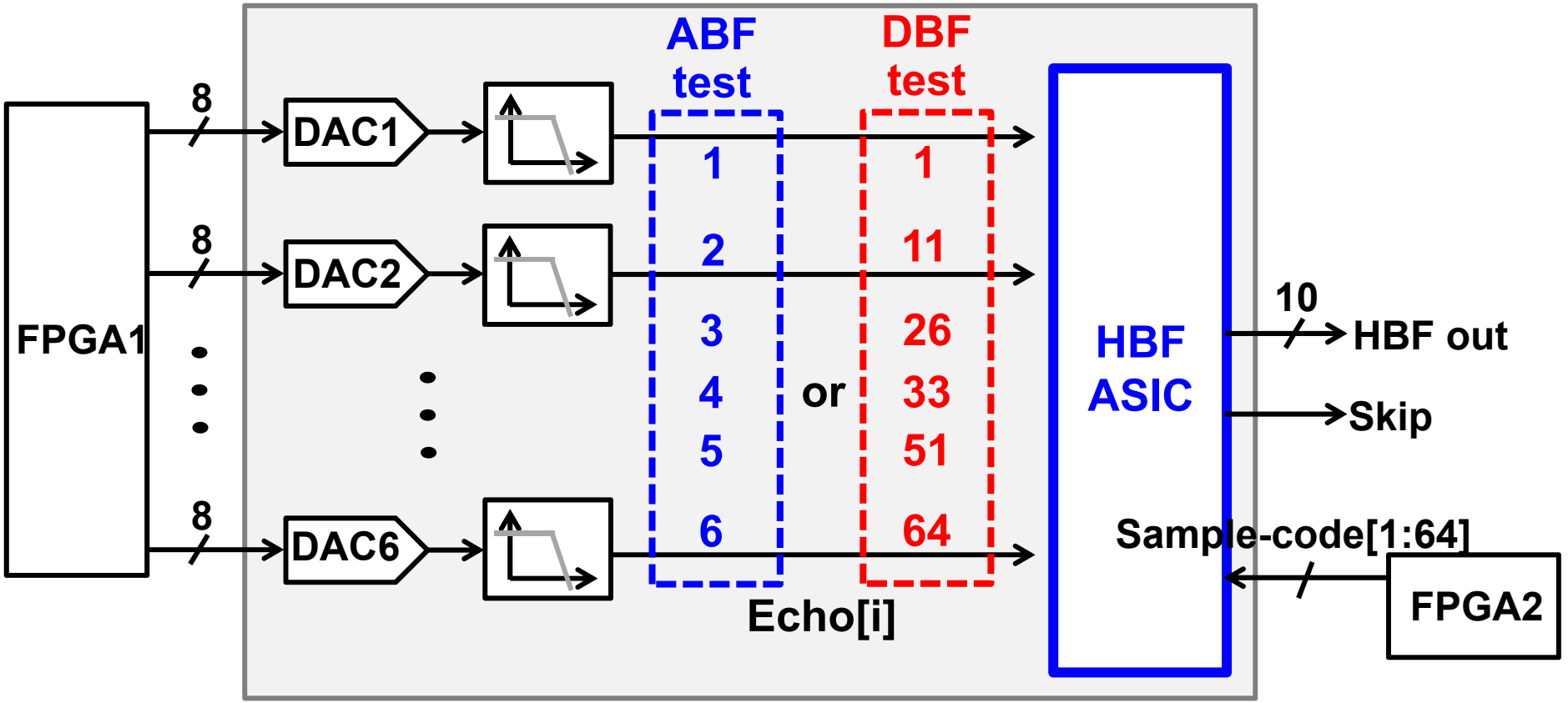
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6-CH Echo Emulation

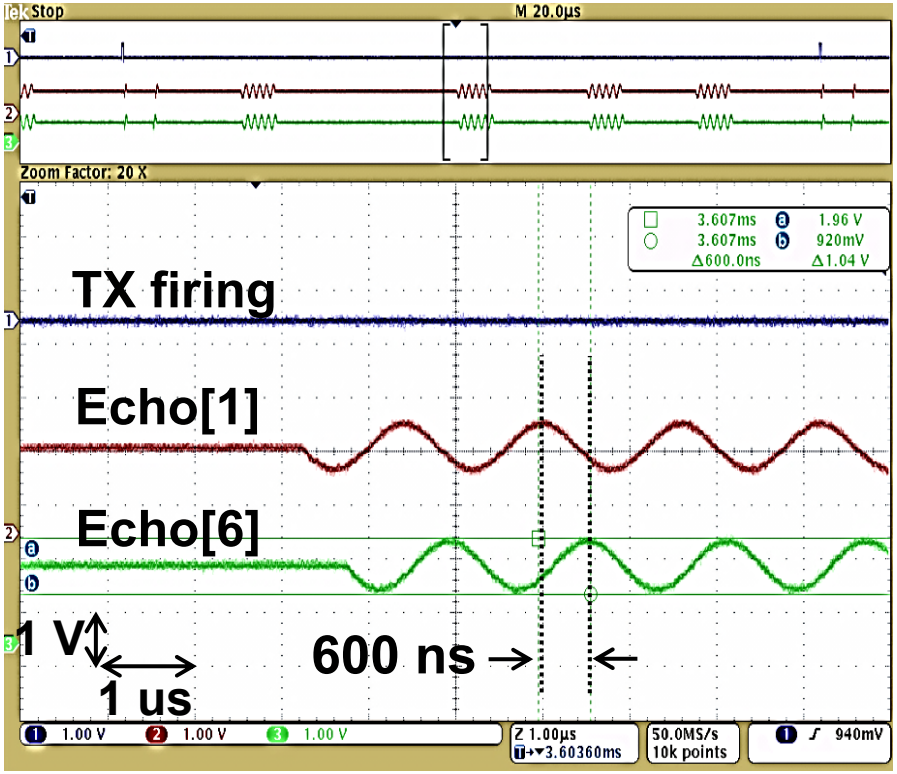


- Test using 6 commercial DAC chips to emulate 6 CH
- Beamforming operations are measured

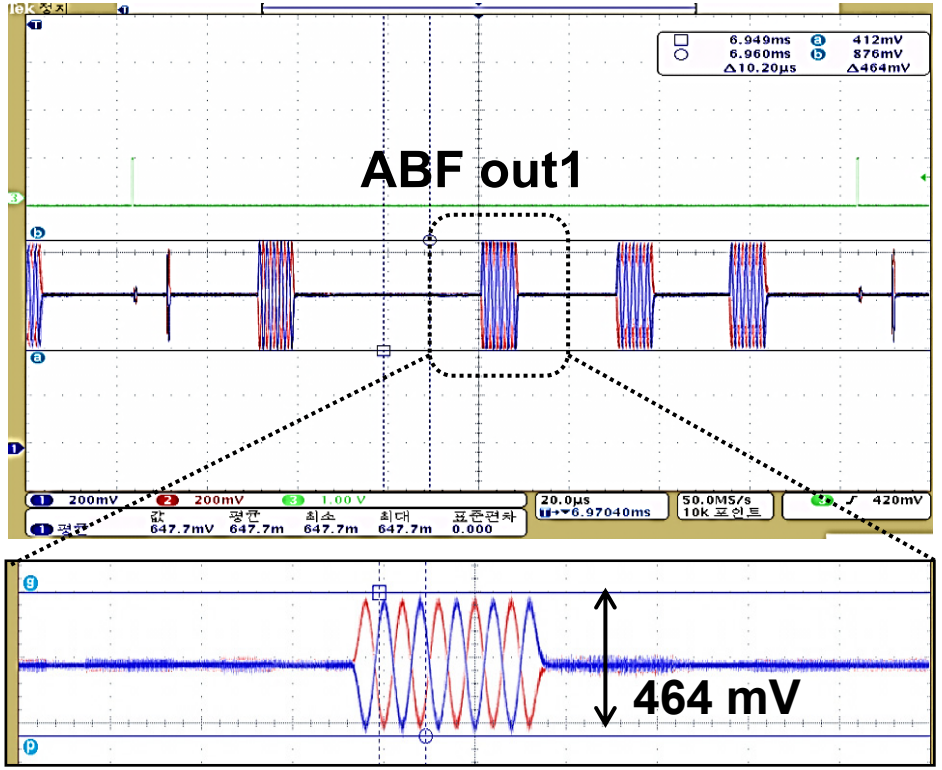
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ABF (6-CH Echo Emulation)

8-CH ABF inputs



8-CH ABF differential outputs

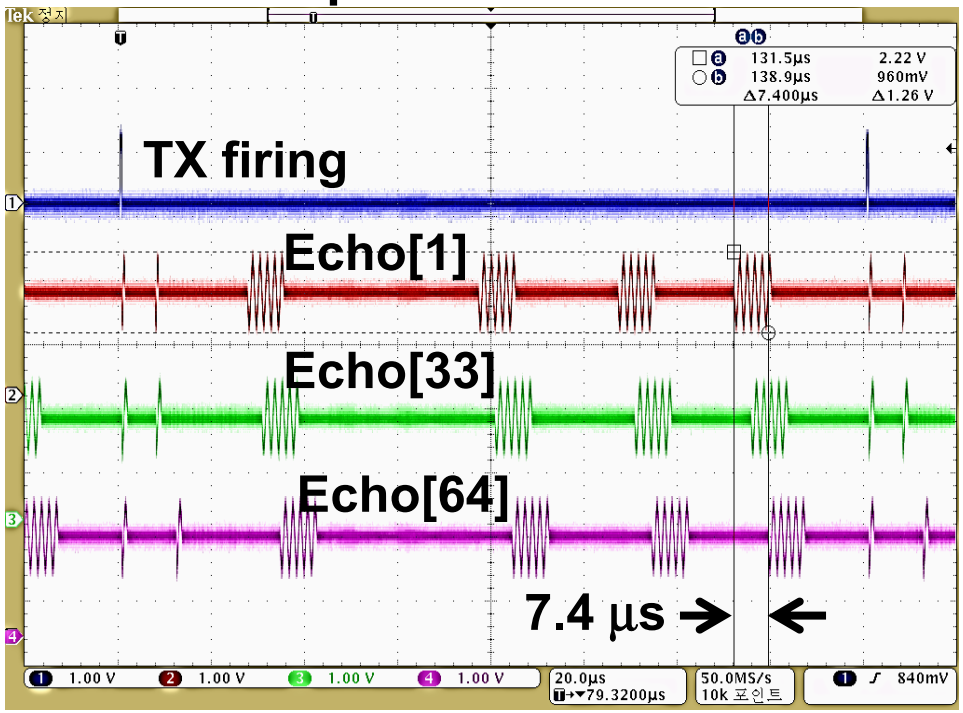


- ABF input : Echo[1:6], sine-waves, linear delay up to 600 ns
- ABF out1 : successfully sums 6 sine-waves as expected (464 mVpp, calculation : 475 mV)

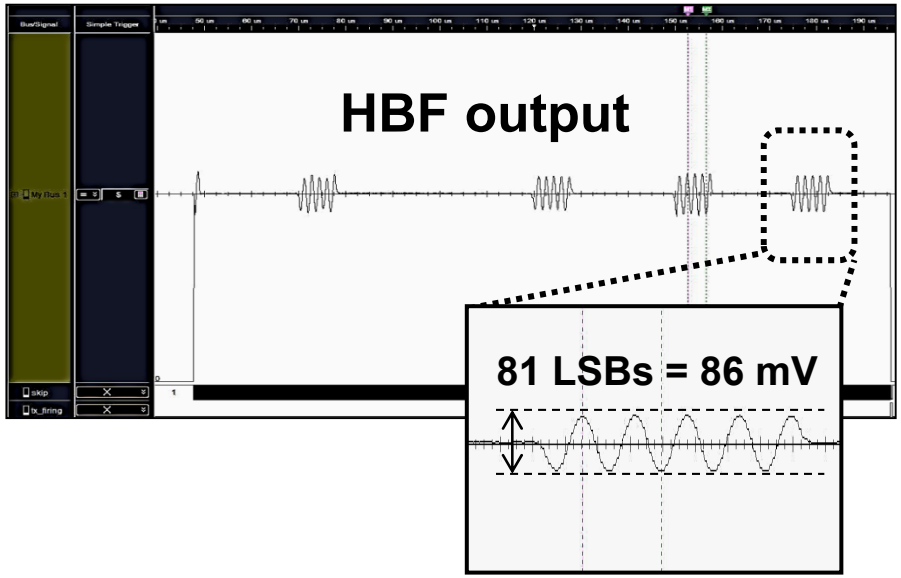
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DBF (6-CH Echo Emulation)

Input waveforms



@ Logic analyzer



- Input : Echo[1, 11, 26, 33, 51, 64], sine-wave, delay up to 7.4 µs
- HBF out : successfully sums 6 sine-waves as expected
 (86 mVpp, calculation : 83 mV)
- Delay profile : emulated a steering angle of 41°

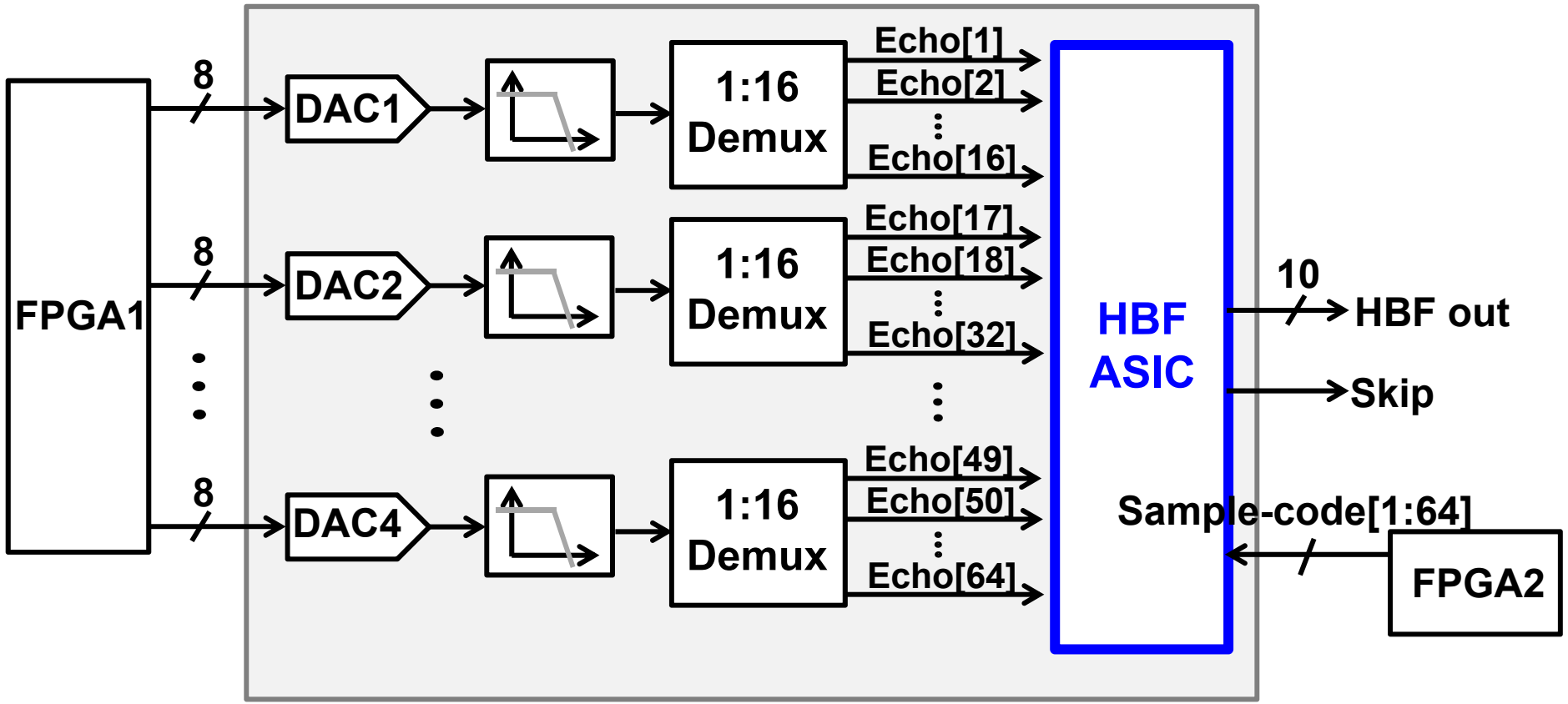
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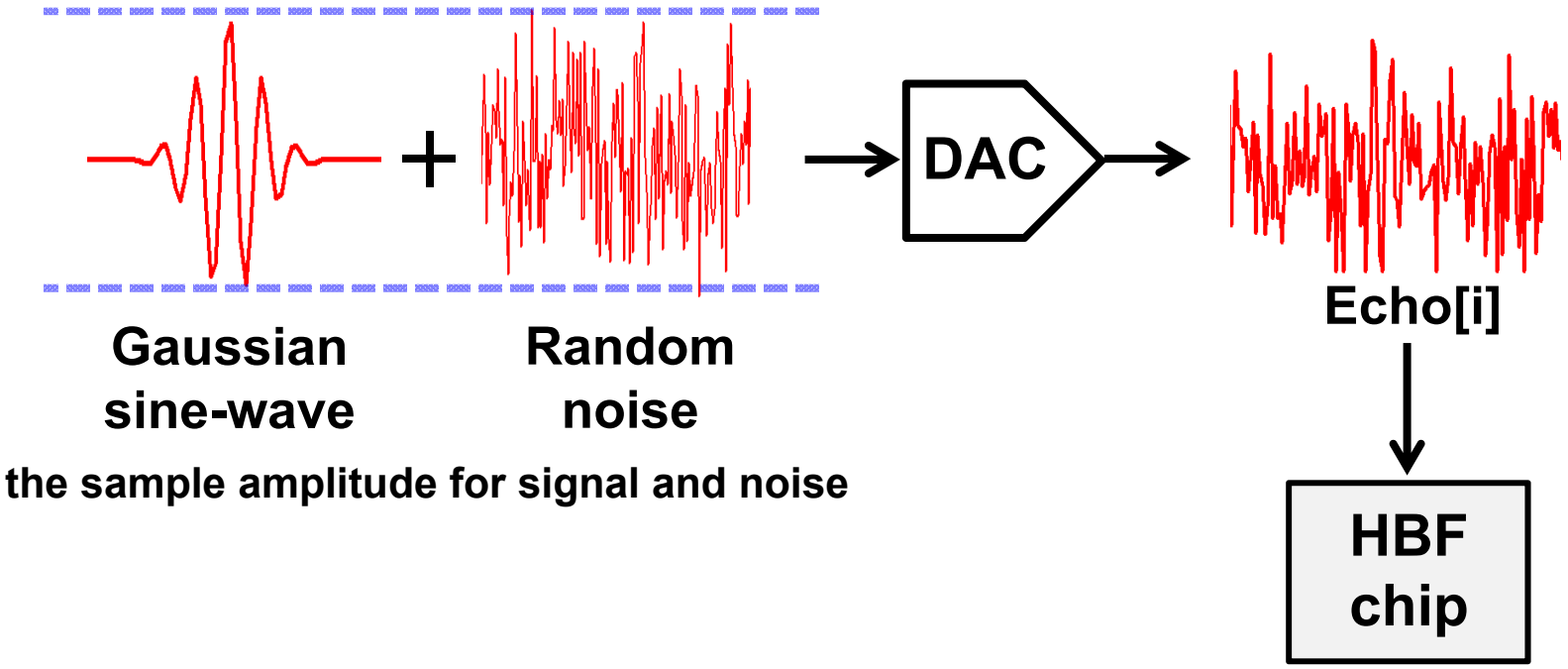
64-CH BF Emulation (1/4)



- Real-time : BF 4 CH at a time (e.g., Echo[1, 17, 33, 49])
- Post-processing : BF 16 real-time outputs for 64 CH BF

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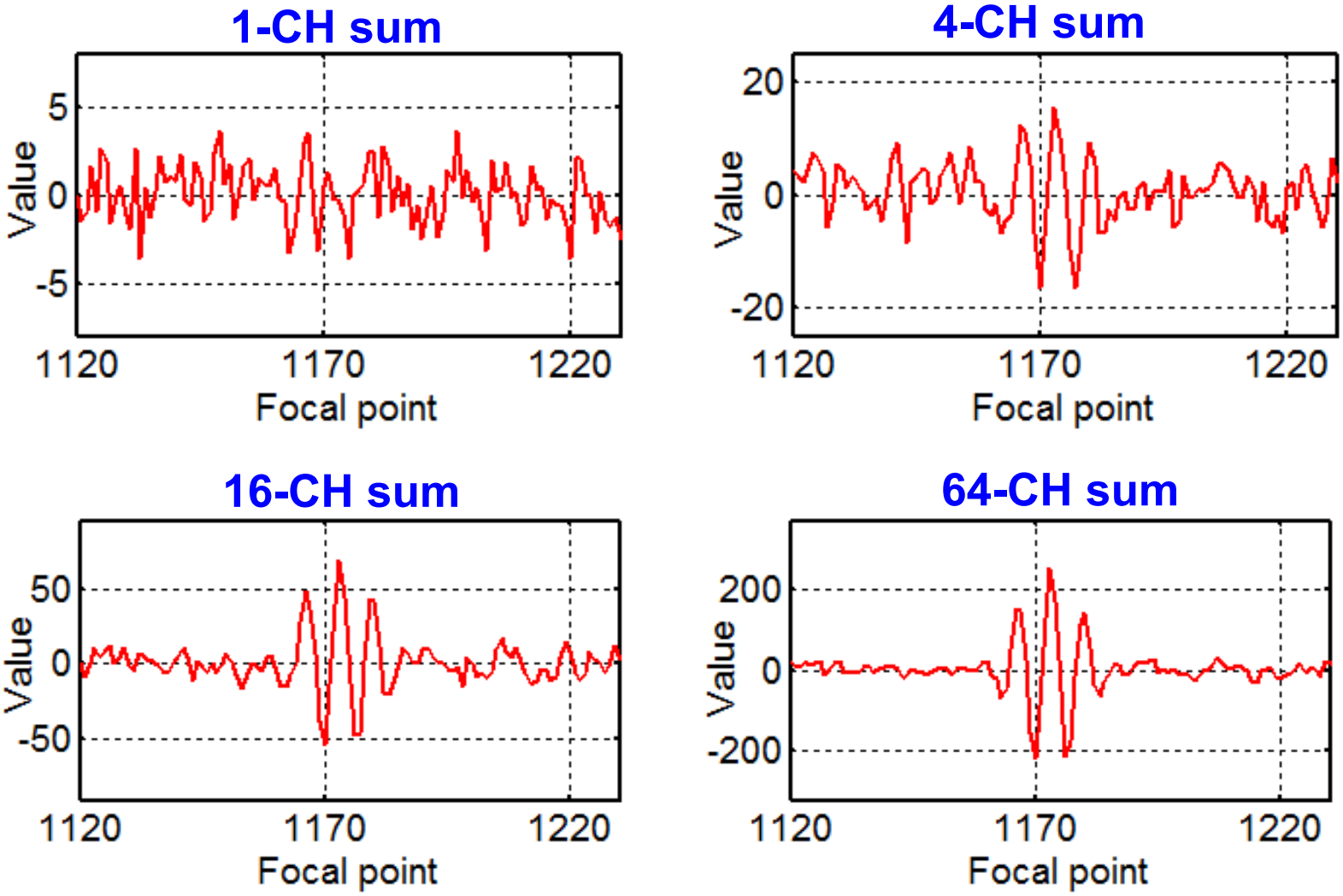
64-CH BF Emulation (2/4)



- For 64 CH BF emulation, random noise added to input
- Delay profile for 45^{o} steering angle used
- Max delay difference : 8 μs

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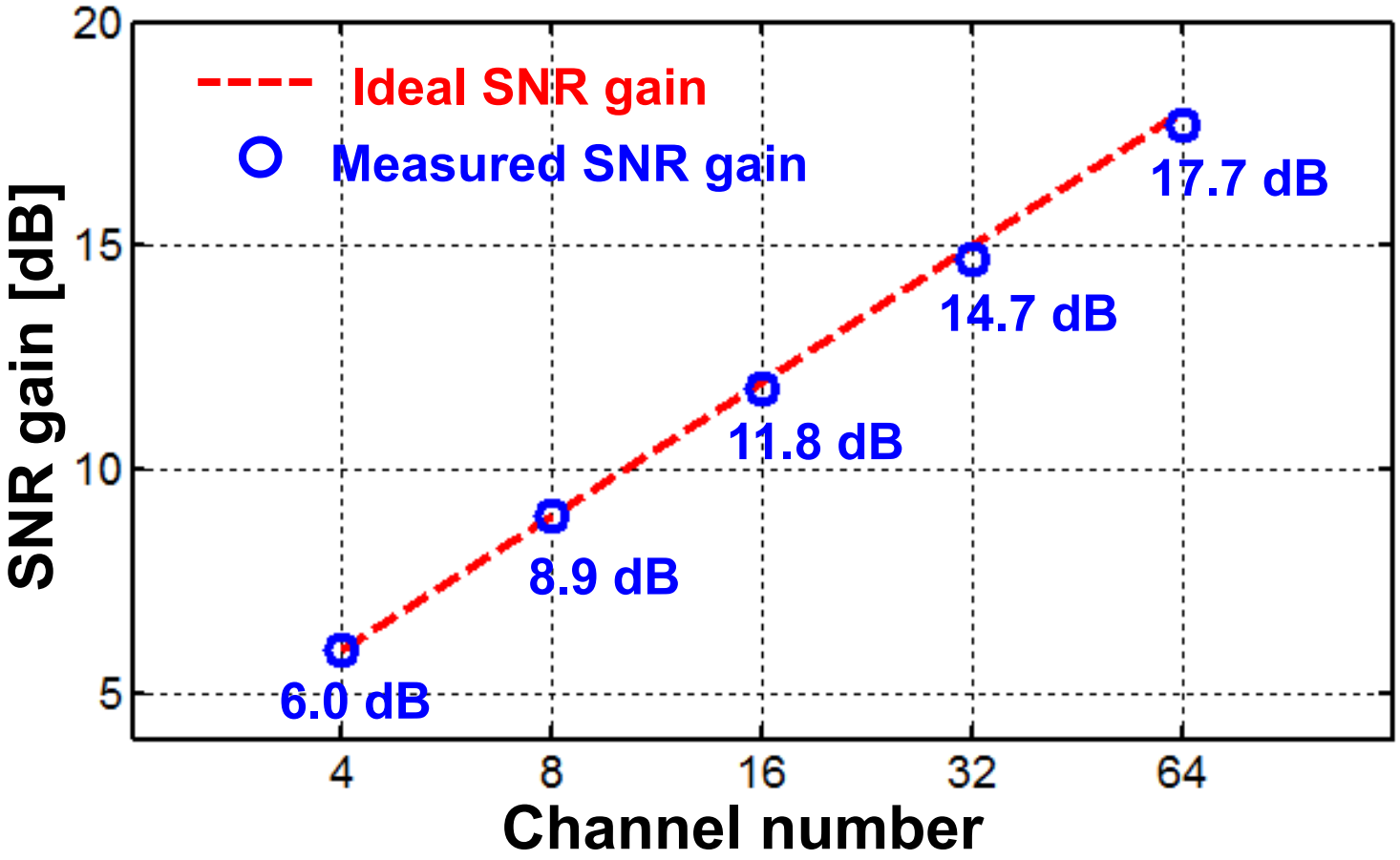
64-CH BF Emulation (3/4)



- **As channel number ↑, signal becomes apparent**

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64-CH BF Emulation (4/4)



- Ideal SNR gain = 10 log (N), N : channel number
- Excellent agreements between meas. & calc.

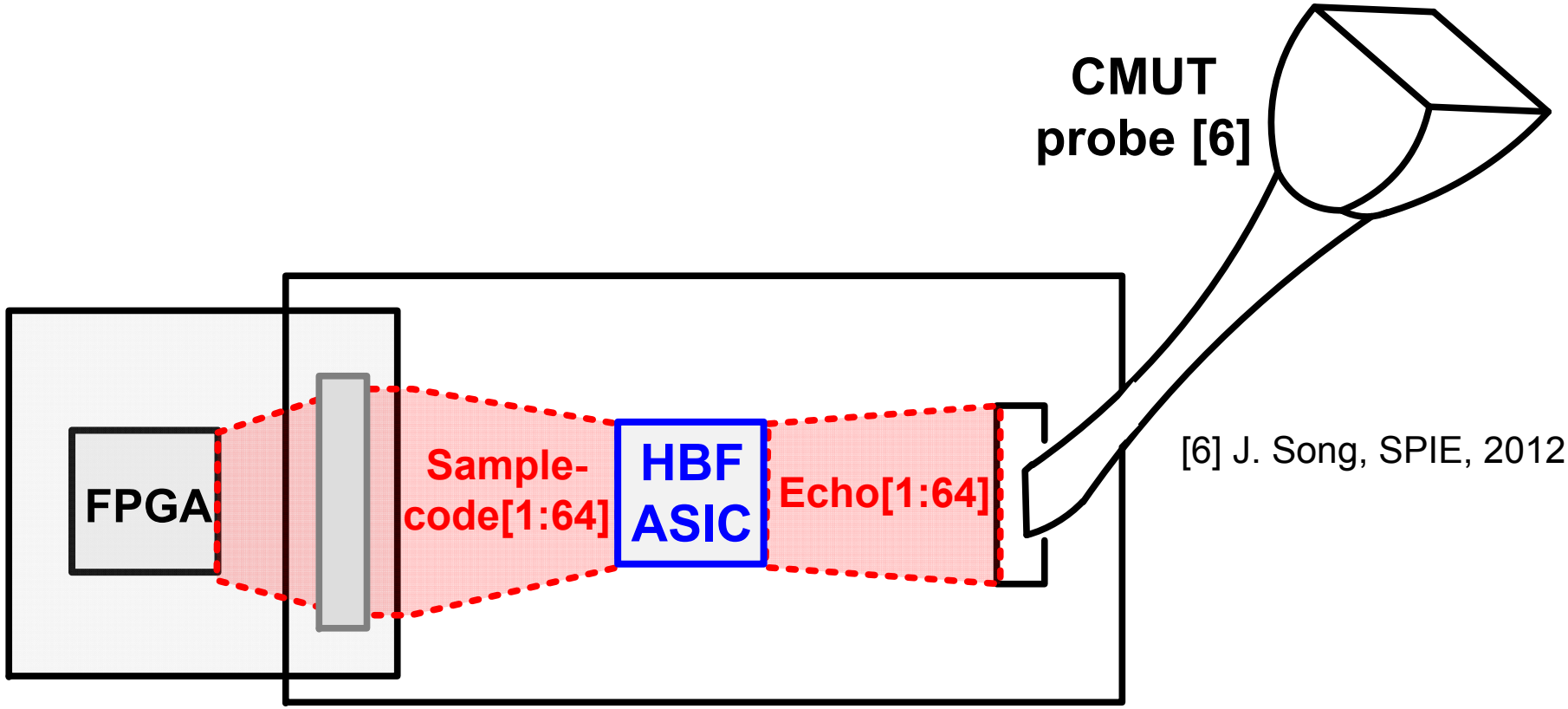
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Outline

- Introduction
- Proposed schemes
- Circuit implementations
- **Measurements**
 - 6CH echo emulation
 - 64CH echo emulation
 - **B-mode image with CMUT probe**
- Conclusion

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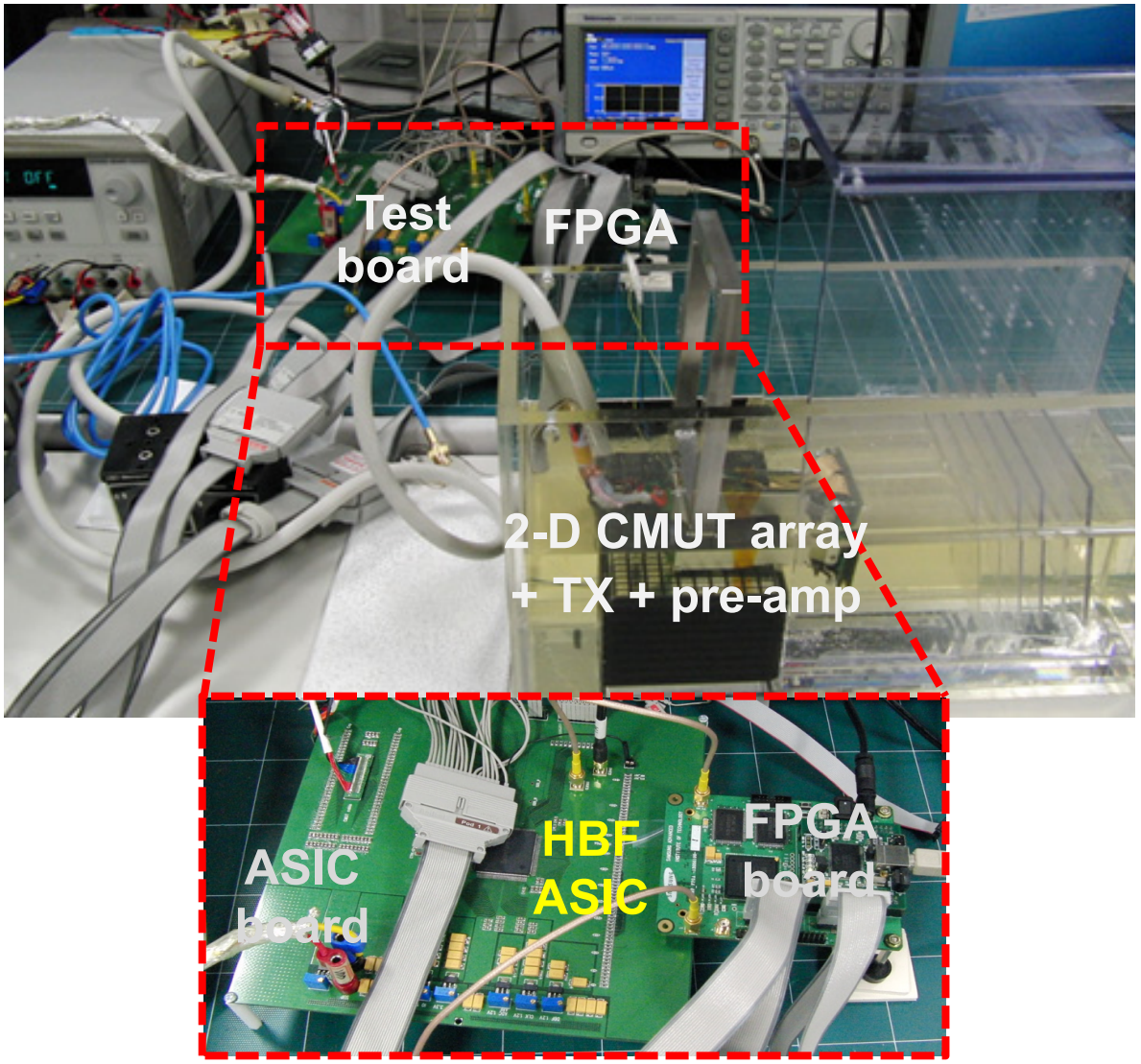
B-mode Image with CMUT Probe (1/4)



- 2D (64 x 128) CMUT probe is used
- 64 echo signals from one row are applied to HBF

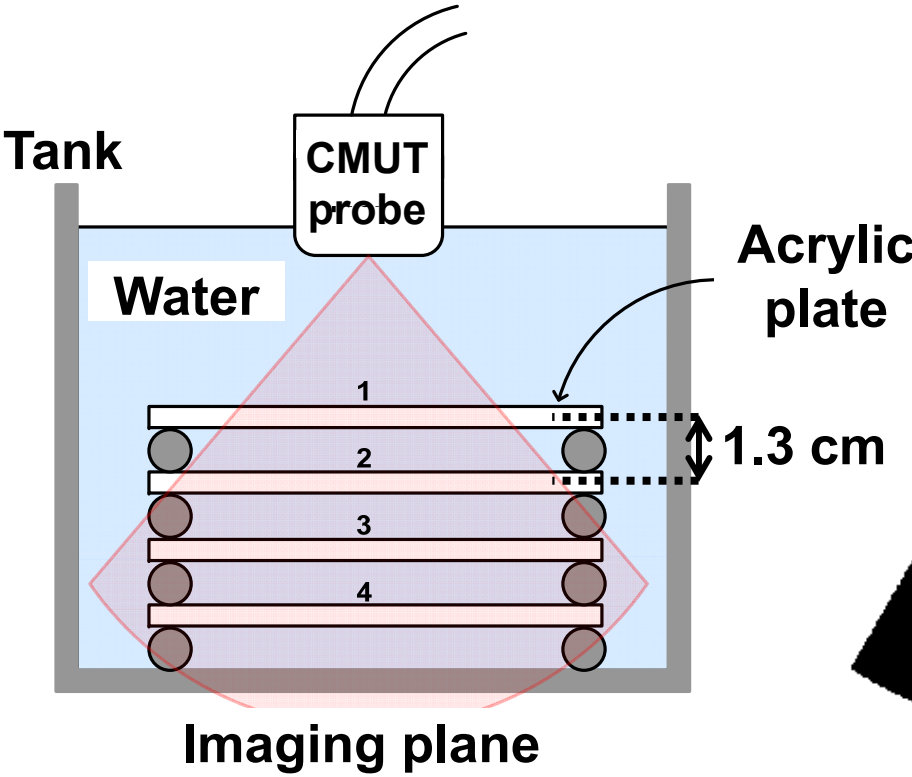
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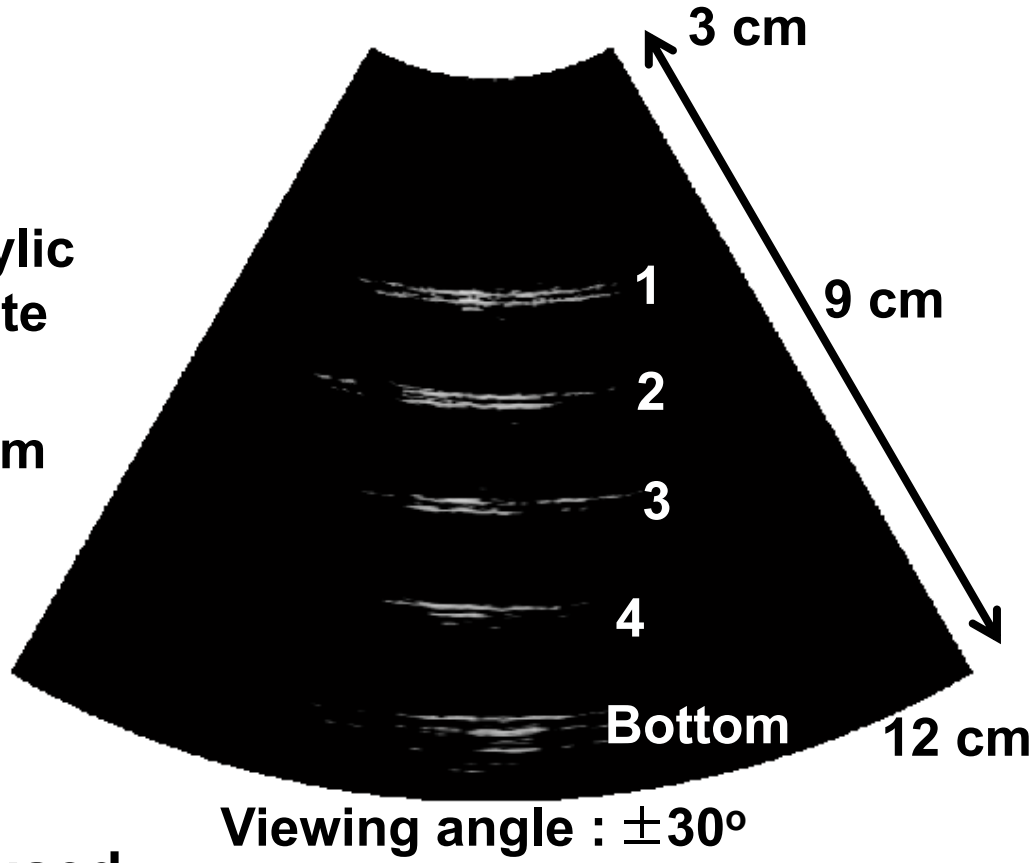
B-mode Image with CMUT Probe (2/4)



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B-mode Image with CMUT Probe (3/4)

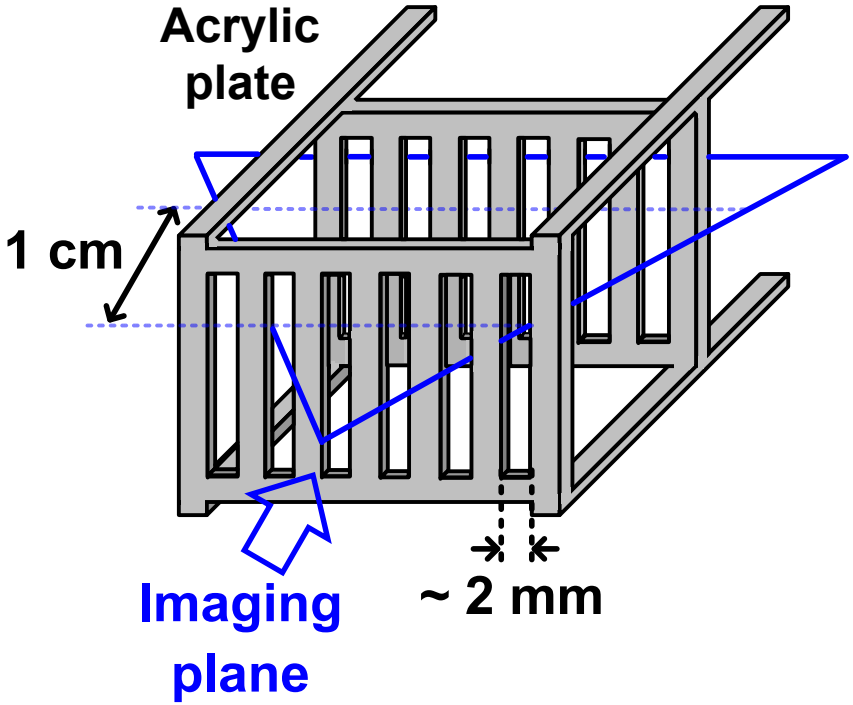


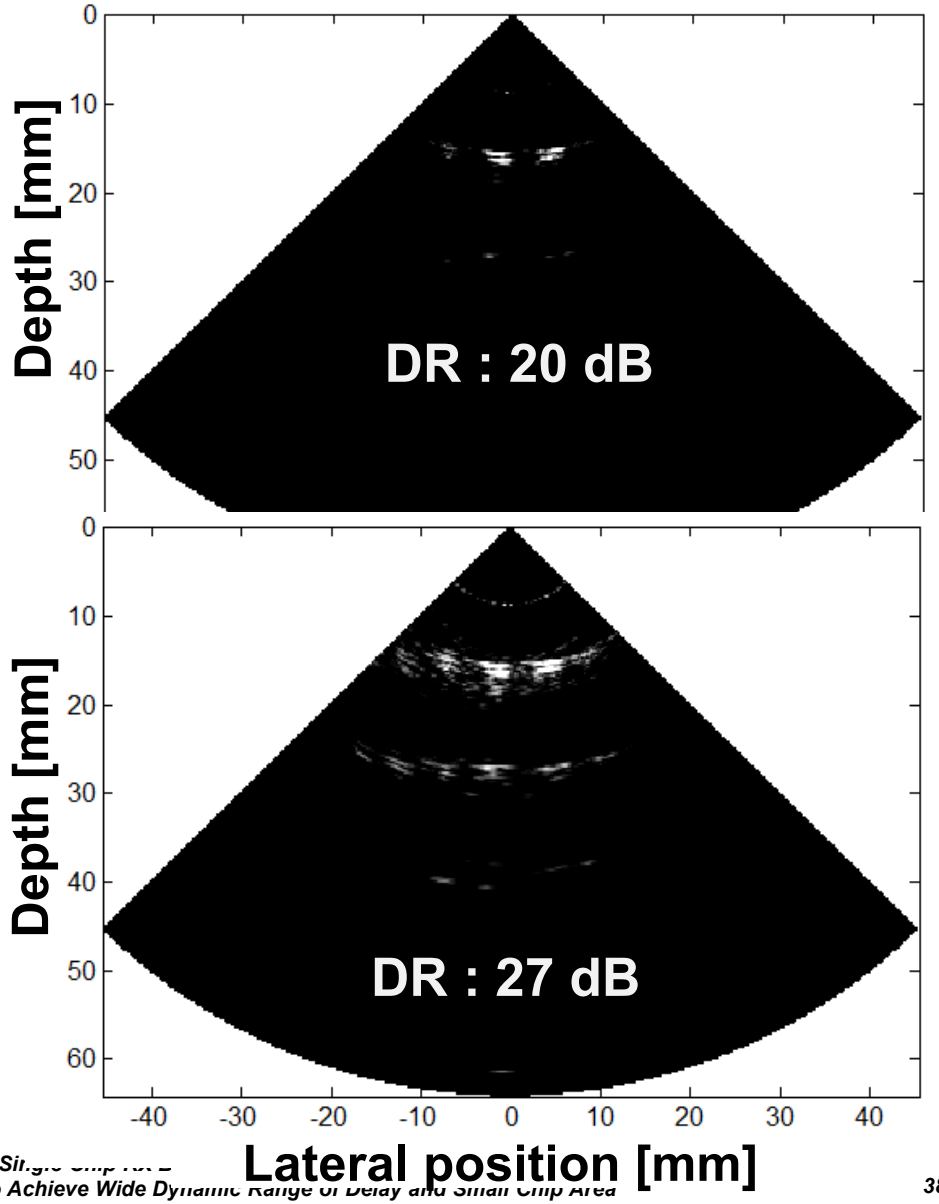


- 4 parallel-plates phantom used
- TX beam : plane wave (un-focused ultrasound wave)
- 4 plates and bottom patterns are clear in US image with image signal DR set to 20 dB

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B-mode Image with CMUT Probe (4/4)





- 2 punched parallel plates phantom
- TX beam : plane wave

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Comparison with Single-Chip BFs

	This work	TBCAS'12	CICC'03	JSSC'00	ASSCC'12
BF type	**Hybrid (analog + digital)**	Analog	Analog	Analog	Analog
Channel #	**64**	8	5	16	32
Delay DR	**1280**	20	55.8	35	192
Power	**1.14 W**	67 mW	N.A.	1.12 W	150 mW
Area	**19.4 mm^2**	0.36 mm^2	0.5 mm^2	72 mm^2	16 mm^2
Process	**0.13 μm**	0.35 μm	0.35 μm	0.8 μm	0.13 μm
FoM^1 [μm^2/CH]	**237**	2250	1792	129000	2604
FoM^2 [μW/CH]	**14**	42	N.A.	2000	25

- **FoM^1 : area for unit delay element per CH =** $\dfrac{Active\ area}{Delay\ DR \times CH\ number}$
- **FoM^2 : power for unit delay element per CH =** $\dfrac{Power}{Delay\ DR \times CH\ number}$
- **The first single-chip hybrid BF**

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Conclusion

- 1 x 64 sub-array BF
 - The first analog-digital-hybrid architecture
 - Non-uniform sampling scheme
 ➔ wide delay dynamic range with small area

- Compared to other single-chip BFs
 - Max. delay DR (1280) & CH number (64)
 - Smaller chip area / (delay DR x CH) by more than 7.5 x

- Measurements of HBF chip
 - Successful real-time BF operation of ABF & DBF
 - Excellent noise suppression through 64CH HBF operation
 - B-mode images acquired with CMUT probe

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